

8

7

6

5

4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV

ZONE

ECN

DESCRIPTION OF CHANGE

CK APPD
DATE

ENG APPD
DATE

03

384363

ENGINEERING RELEASED

06/03/05

?

STD

MARIAS

EVT

PDF

CSA

CONTENTS

SYNC MASTER

DATE

1

1

Table Of Contents

N/A

N/A

2

2

Board Information

N/A

N/A

3

3

System Block Diagram

N/A

N/A

4

4

Power Block Diagram

N/A

N/A

5

5

Revision History

N/A

N/A

6

6

Q16C Pin Swaps

N/A

N/A

7

7

Functional Test Points

N/A

N/A

8

8

I2C Connections

N/A

N/A

9

9

JTAG Connections

N/A

N/A

10

10

Power Synonyms

N/A

N/A

11

11

Signal Synonyms

N/A

N/A

12

12

Power Inputs

N/A

N/A

13

13

Battery Charger

N/A

N/A

14

14

12.8V PBUS/PMU Supplies

N/A

N/A

15

15

5V/3.3V Supplies

N/A

N/A

16

16

1.8V/1.5V Supplies

N/A

N/A

17

17

2.5V Supply

N/A

N/A

18

19

Vesta Power & Misc

N/A

N/A

19

21

I2 Power

N/A

N/A

20

22

I2 Power Supplies

N/A

N/A

21

23

I2 Supplemental

N/A

N/A

22

24

I2 Miscellaneous

N/A

N/A

23

25

PCI Clock Buffer

N/A

N/A

24

26

LEDs/Reset/Debug

N/A

N/A

25

27

Power Management Unit (PMU05)

N/A

N/A

26

29

Power Sequencing

N/A

N/A

27

30

Fan Controller

N/A

N/A

28

31

ALS Support

N/A

N/A

29

32

Sudden Motion Sensor

N/A

N/A

30

33

Q16C Internal I/O I

N/A

N/A

31

34

Q16C Internal I/O II

N/A

N/A

32

35

I2 Processor Interface

N/A

N/A

33

36

A8 MaxBus (CPU0)

MULLET

05/25/2005

34

37

A8 Configuration Straps

MULLET

05/25/2005

35

38

A8 Power (CPU0)

MULLET

05/25/2005

36

39

CPU VCore Supply

N/A

N/A

37

46

CPU AVDD Supply

N/A

N/A

38

47

I2 Memory Interface

N/A

N/A

39

48

Memory Series Termination

N/A

N/A

40

50

DDR2 SO-DIMM Slot A

N/A

N/A

PDF

CSA

CONTENTS

SYNC MASTER

DATE

41

52

DDR2 SO-DIMM Slot B

N/A

N/A

42

55

M11 Frame Buffer Constraints

N/A

N/A

43

56

I2 AGP Interface

N/A

N/A

44

57

GPU (M11) AGP Interface

N/A

N/A

45

58

GPU VCore Supply

N/A

N/A

46

59

GPU (M11) Core Power

N/A

N/A

47

60

GPU (M11) I/O Power

N/A

N/A

48

61

GPU (M11) Frame Buffer I/F

N/A

N/A

49

62

GPU Frame Buffer A

N/A

N/A

50

63

GPU Frame Buffer B

N/A

N/A

51

64

GPU (M11) GPIOs/Straps

N/A

N/A

52

65

GPU (M11) Clocks/Misc

N/A

N/A

53

66

GPU (M11) DVI/DAC Outputs

N/A

N/A

54

67

Lower TMDS Transmitter

N/A

N/A

55

68

Upper TMDS Transmitter

N/A

N/A

56

69

Internal Display Conns

N/A

N/A

57

70

External Display Conns

N/A

N/A

58

71

BootROM

N/A

N/A

59

72

I2 PCI Interface

N/A

N/A

60

73

Q85 Airport/BT Connector

N/A

N/A

61

74

Cardbus

N/A

N/A

62

75

NEC USB2

N/A

N/A

63

81

I2 UATA Interface

N/A

N/A

64

82

HDD/ODD Connectors

N/A

N/A

65

84

I2 Ethernet Interface

N/A

N/A

66

85

Vesta Ethernet PHY

N/A

N/A

67

86

Ethernet Connector

N/A

N/A

68

88

I2 FireWire Interface

N/A

N/A

69

89

Vesta FireWire PHY

N/A

N/A

70

90

FireWire Ports

N/A

N/A

71

91

FireWire Series Term

N/A

N/A

72

92

I2 USB Interface

N/A

N/A

73

93

NEC USB2 Interface

N/A

N/A

74

100

Audio Board Connector

N/A

N/A

75

110

Spacing & Physical Constraints

N/A

N/A

76

111

Spacing & Physical Constraints 2

N/A

N/A

77

112

Cross Reference Page

78

113

Cross Reference Page

79

114

Cross Reference Page

80

115

Cross Reference Page

PART#

QTY

DESCRIPTION

REFERENCE DESIGNATOR(S)

BOM OPTION

051-6929

1

SCHEM,MARIAS-STD,Q16C

SCH1

820-1875

1

PCBF,MARIAS,12L-STD,Q16C

PCB1

826-4393

1

LBL,P/N LABEL,PCB,28MM x 6MM

[EEE:SYT]

Q16C_BTR_VRAM_S

826-4393

1

LBL,P/N LABEL,PCB,28MM x 6MM

[EEE:SYU]

Q16C_BST_VRAM_S

826-4393

1

LBL,P/N LABEL,PCB,28MM x 6MM

[EEE:TMJ]

Q16C_BTR_VRAM_H

826-4393

1

LBL,P/N LABEL,PCB,28MM x 6MM

[EEE:TMK]

Q16C_BST_VRAM_H

DIMENSIONS ARE IN MILLIMETERS

XX ±

X.XX ±

X.XXX ±

ANGLES ±

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER

ENG APPD

QA APPD

RELEASE

DESIGN CK

MFG APPD

DESIGNER

SCALE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE

NONE

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TITLE

SCHEM,MARIAS-STD,Q16C

DRAWING NUMBER

051-6929

REV.

03

SHT

1

OF

115

8

7

6

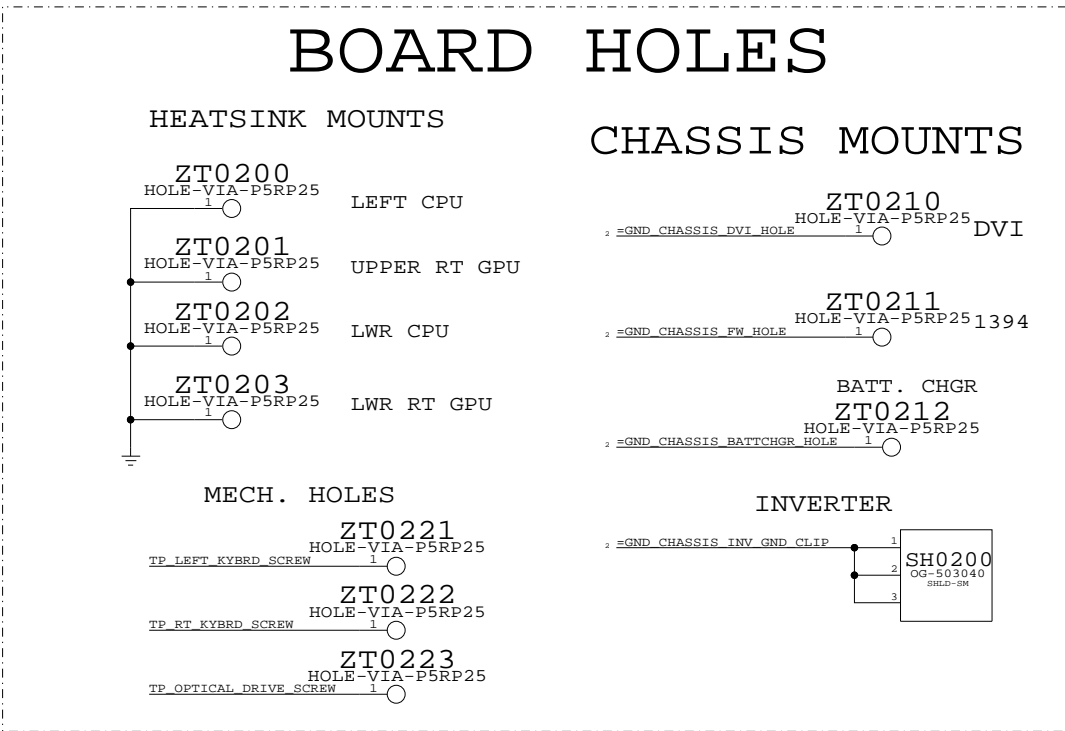
5

4

3

2

1

[illegible]

SEE BOARD FILE FOR DETAILED INFORMATION
CONVENTIONAL CONSTRUCTION WITH Pxx TH VIA

TABLE_BOARD_INFO		
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, 1MM	MM

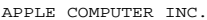
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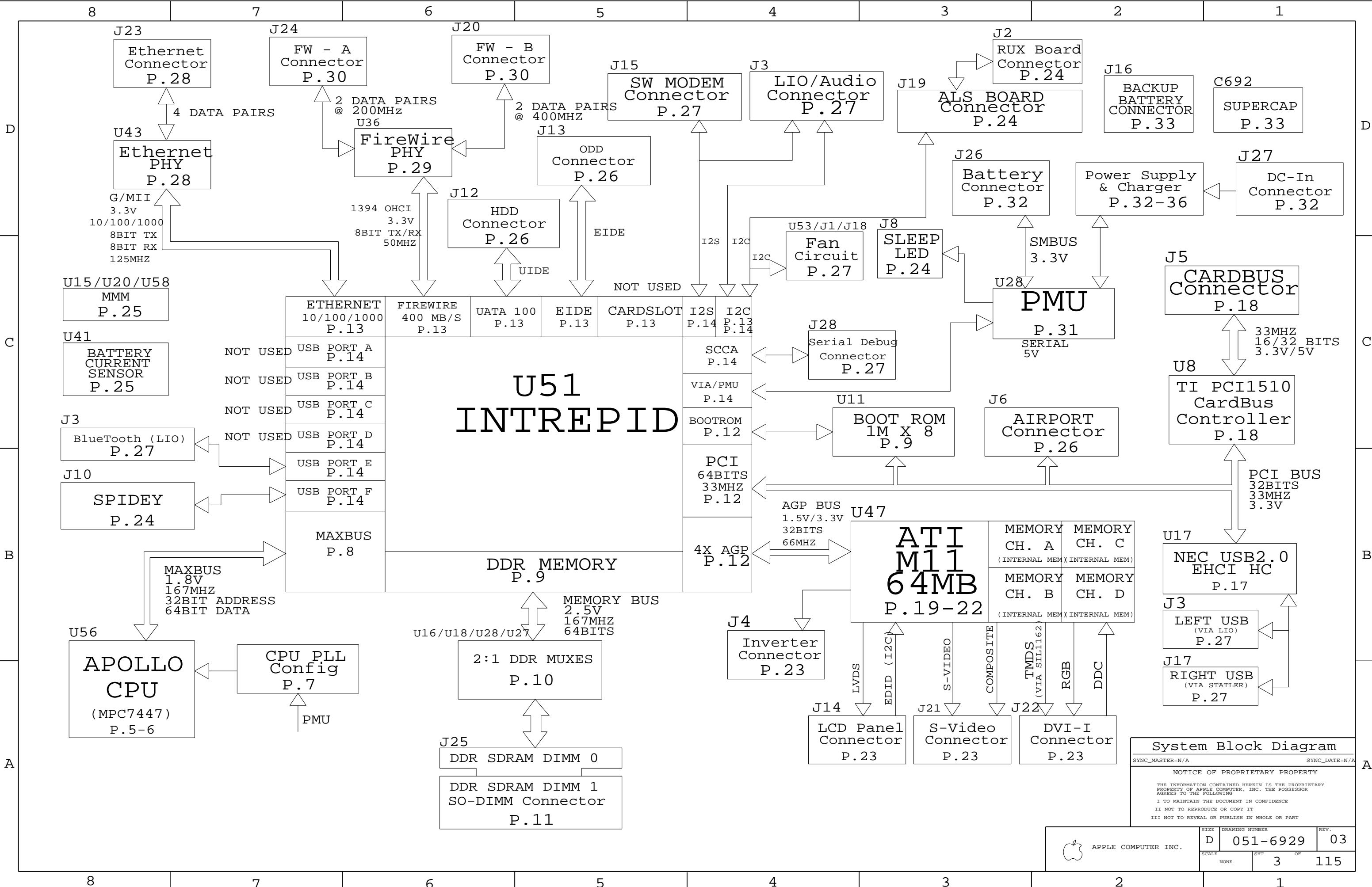
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SIZE	DRAWING NUMBER		REV.
D	051-6929		0
SCALE		SHT	OF
NONE		2	115



System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

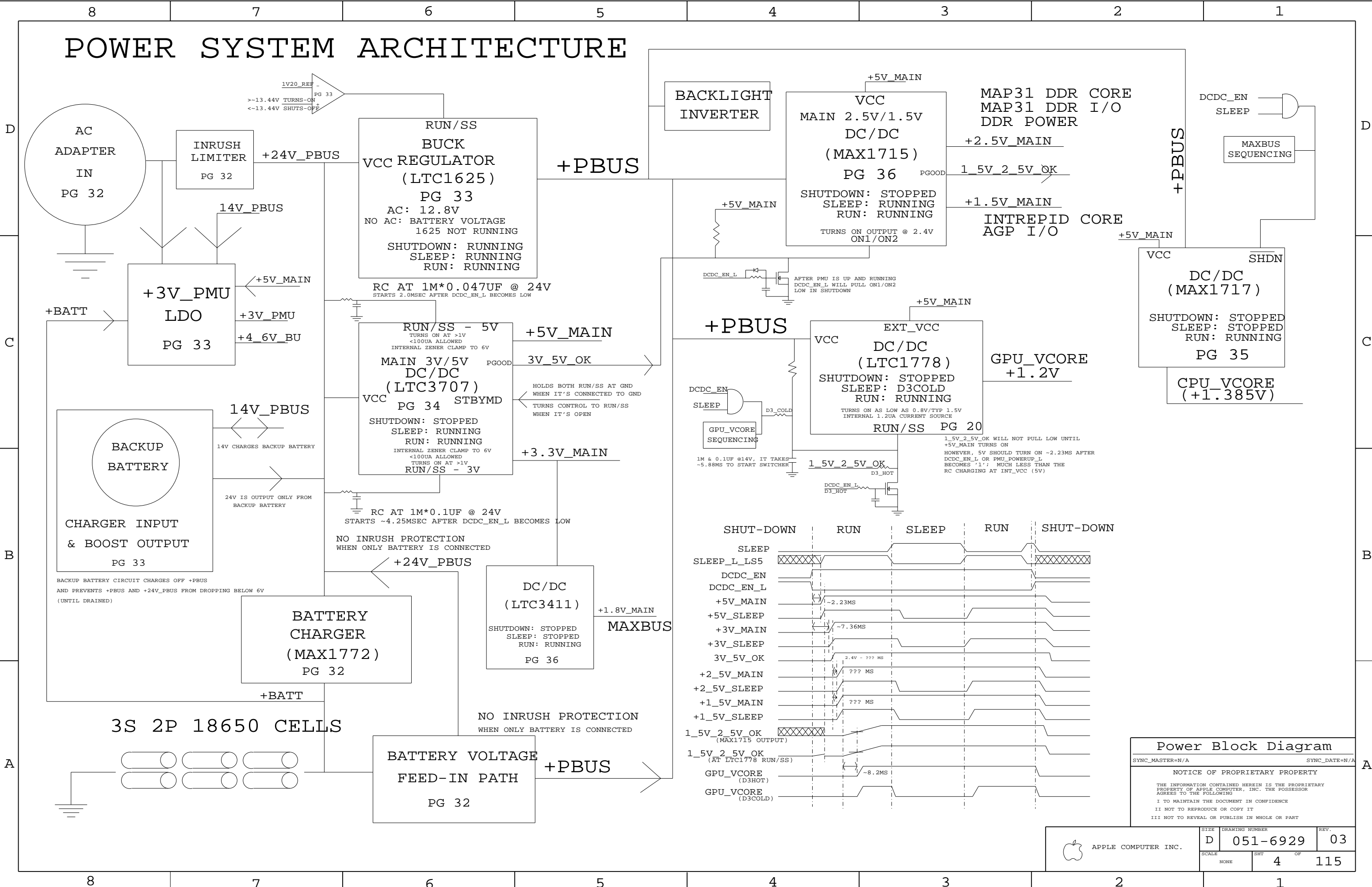
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	8	7	6	5	4	3	2	1	
D	<div>I2S Series Rs</div> <div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S0_SB_TO_DEV_DTO_R</div><div>==</div><div>=RP1150P1</div><div>11</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S0_BITCLK_R</div><div>==</div><div>=RP1150P2</div><div>11</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S0_MCLK_R</div><div>==</div><div>=RP1150P3</div><div>11</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S0_SYNC_R</div><div>==</div><div>=RP1150P4</div><div>11</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S1_SB_TO_DEV_DTO_R</div><div>==</div><div>=RP1151P1</div><div>11</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S1_SYNC_R</div><div>==</div><div>=RP1151P2</div><div>11</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S1_MCLK_R</div><div>==</div><div>=RP1151P3</div><div>11</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S1_BITCLK_R</div><div>==</div><div>=RP1151P4</div><div>11</div></div><div><div><div>=RP1150P8</div><div>11</div><div>I2S0_SB_TO_DEV_DTO</div><div>7</div><div>74</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S0_BITCLK</div><div>7</div><div>74</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S0_MCLK</div><div>7</div><div>74</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S0_SYNC</div><div>7</div><div>74</div></div><div><div><div>=RP1151P8</div><div>11</div><div>I2S1_SB_TO_DEV_DTO</div><div>30</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S1_SYNC</div><div>30</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S1_MCLK</div><div>30</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S1_BITCLK</div><div>30</div></div><div><div><div>=RP1151P5</div><div>11</div><div>I2S1_BITCLK</div><div>30</div></div><div><div>MAKE_BASE=TRUE</div><div>22</div><div>I2S1_BITCLK</div><div>30</div></div></div></div><div>Lower DVO Series Rs</div><div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<16></div><div>==</div><div>=RP6720P1</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<4></div><div>==</div><div>=RP6720P2</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<7></div><div>==</div><div>=RP6720P3</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<6></div><div>==</div><div>=RP6720P4</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<11></div><div>==</div><div>=RP6721P1</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<9></div><div>==</div><div>=RP6721P2</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<10></div><div>==</div><div>=RP6721P3</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVO_HSYNC_R</div><div>==</div><div>=RP6721P4</div><div>54</div></div><div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<3></div><div>==</div><div>=RP6722P1</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<5></div><div>==</div><div>=RP6722P2</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<13></div><div>==</div><div>=RP6722P3</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<12></div><div>==</div><div>=RP6722P4</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<2></div><div>==</div><div>=RP6723P1</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<1></div><div>==</div><div>=RP6723P2</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<0></div><div>==</div><div>=RP6723P3</div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<14></div><div>==</div><div>=RP6723P4</div><div>54</div></div><div><div><div>=RP6720P8</div><div>54</div><div>GPU_DVOD<16></div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<4></div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<7></div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<6></div><div>54</div></div><div><div><div>=RP6721P8</div><div>54</div><div>GPU_DVOD<11></div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<9></div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<10></div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVO_HSYNC</div><div>54</div><div>55</div></div><div><div><div>=RP6722P8</div><div>54</div><div>GPU_DVOD<3></div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<5></div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<13></div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<12></div><div>54</div></div><div><div><div>=RP6723P8</div><div>54</div><div>GPU_DVOD<2></div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<1></div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<0></div><div>54</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<14></div><div>54</div></div></div></div></div></div></div></div></div></div>								D
C	<div>UATA Series Rs</div> <div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<12></div><div>==</div><div>=RP8150P1</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_CS0_L_R</div><div>==</div><div>=RP8150P2</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<14></div><div>==</div><div>=RP8150P3</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<11></div><div>==</div><div>=RP8150P4</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<7></div><div>==</div><div>=RP8151P1</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<2></div><div>==</div><div>=RP8151P2</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<3></div><div>==</div><div>=RP8151P3</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<15></div><div>==</div><div>=RP8151P4</div><div>63</div></div><div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<9></div><div>==</div><div>=RP8152P1</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<4></div><div>==</div><div>=RP8152P2</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<6></div><div>==</div><div>=RP8152P3</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<5></div><div>==</div><div>=RP8152P4</div><div>63</div></div><div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DA_R<2></div><div>==</div><div>=RP8153P1</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<8></div><div>==</div><div>=RP8153P2</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<10></div><div>==</div><div>=RP8153P3</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DA_R<0></div><div>==</div><div>=RP8153P4</div><div>63</div></div><div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<13></div><div>==</div><div>=RP8154P1</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<0></div><div>==</div><div>=RP8154P2</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD_R<1></div><div>==</div><div>=RP8154P3</div><div>63</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DA_R<1></div><div>==</div><div>=RP8154P4</div><div>63</div></div><div><div><div>=RP8150P8</div><div>63</div><div>UATA_DD<12></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_CS0_L</div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<14></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<11></div><div>7</div><div>63</div><div>64</div></div><div><div><div>=RP8151P8</div><div>63</div><div>UATA_DD<7></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<2></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<3></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<15></div><div>7</div><div>63</div><div>64</div></div><div><div><div>=RP8152P8</div><div>63</div><div>UATA_DD<9></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<4></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<6></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<5></div><div>7</div><div>63</div><div>64</div></div><div><div><div>=RP8153P8</div><div>63</div><div>UATA_DA<2></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<8></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<10></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DA<0></div><div>7</div><div>63</div><div>64</div></div><div><div><div>=RP8154P8</div><div>63</div><div>UATA_DD<13></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<0></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<1></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DA<1></div><div>7</div><div>63</div><div>64</div></div><div><div><div>=RP8150P5</div><div>63</div><div>UATA_DD<11></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<11></div><div>7</div><div>63</div><div>64</div></div><div><div><div>=RP8151P5</div><div>63</div><div>UATA_DD<15></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<15></div><div>7</div><div>63</div><div>64</div></div><div><div><div>=RP8152P5</div><div>63</div><div>UATA_DD<5></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<5></div><div>7</div><div>63</div><div>64</div></div><div><div><div>=RP8153P5</div><div>63</div><div>UATA_DA<0></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DD<10></div><div>7</div><div>63</div><div>64</div></div><div><div><div>=RP8154P5</div><div>63</div><div>UATA_DA<1></div><div>7</div><div>63</div><div>64</div></div><div><div>MAKE_BASE=TRUE</div><div>63</div><div>UATA_DA<1></div><div>7</div><div>63</div><div>64</div></div></div></div></div></div><div>(IDE_CS1FX_L)</div><div>Upper DVO Series Rs</div><div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVO_DE_R</div><div>==</div><div>=RP6821P1</div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVO_VSYNC_R</div><div>==</div><div>=RP6821P2</div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVO_CLKP_R</div><div>==</div><div>=RP6821P3</div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<8></div><div>==</div><div>=RP6821P4</div><div>55</div></div><div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<21></div><div>==</div><div>=RP6822P1</div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<19></div><div>==</div><div>=RP6822P2</div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<17></div><div>==</div><div>=RP6822P3</div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<15></div><div>==</div><div>=RP6822P4</div><div>55</div></div><div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<20></div><div>==</div><div>=RP6823P1</div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<22></div><div>==</div><div>=RP6823P2</div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<23></div><div>==</div><div>=RP6823P3</div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD_R<18></div><div>==</div><div>=RP6823P4</div><div>55</div></div><div><div><div>=RP6821P8</div><div>55</div><div>GPU_DVO_DE</div><div>54</div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVO_VSYNC</div><div>54</div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVO_CLKP</div><div>54</div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<8></div><div>54</div></div><div><div><div>=RP6822P8</div><div>55</div><div>GPU_DVOD<21></div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<19></div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<17></div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<15></div><div>55</div></div><div><div><div>=RP6823P8</div><div>55</div><div>GPU_DVOD<20></div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<22></div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<23></div><div>55</div></div><div><div>MAKE_BASE=TRUE</div><div>53</div><div>GPU_DVOD<18></div><div>55</div></div></div></div></div></div></div></div></div></div></div></div></div></div></div></div></div></div>								C
B	<div>MAXBUS Pullups</div> <div><div><div>MAKE_BASE=TRUE</div><div>33</div><div>MAXBUS_TS_L</div><div>==</div><div>=RP3510P1</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>32</div><div>MAXBUS_CPU1_BG_L</div><div>==</div><div>=RP3510P2</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>33</div><div>MAXBUS_CPU0_DBG_L</div><div>==</div><div>=RP3510P3</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>32</div><div>MAXBUS_TBNEN_I2</div><div>==</div><div>=RP3510P4</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>33</div><div>MAXBUS_CPU0_BG_L</div><div>==</div><div>=RP3511P1</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>32</div><div>MAXBUS_CPU1_HIT_L</div><div>==</div><div>=RP3511P2</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>33</div><div>MAXBUS_CPU0_HIT_L</div><div>==</div><div>=RP3511P3</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>33</div><div>MAXBUS_CPU0_BR_L</div><div>==</div><div>=RP3511P4</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>32</div><div>MAXBUS_CPU1_BR_L</div><div>==</div><div>=RP3512P1</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>33</div><div>MAXBUS_TA_L</div><div>==</div><div>=RP3512P2</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>34</div><div>MAXBUS_CPU0_INT_L</div><div>==</div><div>=RP3512P3</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>32</div><div>MAXBUS_CPU1_INT_L</div><div>==</div><div>=RP3512P4</div><div>32</div></div><div><div><div>MAKE_BASE=TRUE</div><div>33</div><div>MAXBUS_CPU0_DRDY_L</div><div>==</div><div>=RP3513P2</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>32</div><div>MAXBUS_CPU1_DRDY_L</div><div>==</div><div>=RP3513P3</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>33</div><div>MAXBUS_AACK_L</div><div>==</div><div>=RP3513P4</div><div>32</div></div><div><div>MAKE_BASE=TRUE</div><div>33</div><div>MAXBUS_ARTRY_L</div><div>==</div><div>=RP</div></div></div></div>								

Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.

POWER	PP24V ADAPTER	10	FUNC_TEST=YES	Place 2 TPs @ connector.
	PP24V ALL PBUSA	10	FUNC_TEST=YES	
	PP12V8 ALL PBUSB	10	FUNC_TEST=YES	
	PPVCORE RUN GPU	10	FUNC_TEST=YES	
	PPVCORE RUN CPU	10	FUNC_TEST=YES	Place within 50 mm of power supply.
	PP1V8 PWRON	10	FUNC_TEST=YES	
	PP2V5 PWRON	10	FUNC_TEST=YES	
	PP5V PWRON	10	FUNC_TEST=YES	
	PP3V3 PWRON	10	FUNC_TEST=YES	Place 5-10 GND TPs.
	PP5V RUN	10	FUNC_TEST=YES	
	PP3V3 ALL	10	FUNC_TEST=YES	
	=FTP GND	7 10	FUNC_TEST=YES	
LVDS	LVDS U0_P	53 56	FUNC_TEST=YES	Place within 25 mm of LVDS connector.
	LVDS U0_N	53 56	FUNC_TEST=YES	
	LVDS U1_P	53 56	FUNC_TEST=YES	
	LVDS U1_N	53 56	FUNC_TEST=YES	
	LVDS U2_P	53 56	FUNC_TEST=YES	
	LVDS U2_N	53 56	FUNC_TEST=YES	
	CLKLVDS U_P	53 56	FUNC_TEST=YES	
	CLKLVDS U_N	53 56	FUNC_TEST=YES	
	LVDS L0_P	53 56	FUNC_TEST=YES	
	LVDS L0_N	53 56	FUNC_TEST=YES	
	LVDS L1_P	53 56	FUNC_TEST=YES	
	LVDS L1_N	53 56	FUNC_TEST=YES	
	LVDS L2_P	53 56	FUNC_TEST=YES	
	LVDS L2_N	53 56	FUNC_TEST=YES	
	CLKLVDS L_P	53 56	FUNC_TEST=YES	
	CLKLVDS L_N	53 56	FUNC_TEST=YES	
INVERTER	PPBUS INVERTER	56	FUNC_TEST=YES	Place within 25 mm of inverter connector.
	PP5V INV SW	56	FUNC_TEST=YES	
	BRIGHT PWM	56	FUNC_TEST=YES	
	GND INVERTER	56	FUNC_TEST=YES	
UATA	=PP5V RUN_ODD	10 64	FUNC_TEST=YES	Place within 50 mm of ODD/HDD connector.
	=PP5V RUN_HDD	10 64	FUNC_TEST=YES	
	PP3V3R5V RUN HDD LOGIC	64	FUNC_TEST=YES	
	UATA_DD<15..0>	6 63 64	FUNC_TEST=YES	
	UATA_DMARQ	63 64	FUNC_TEST=YES	
	UATA_DSTROBE	63 64	FUNC_TEST=YES	
	UATA_DMACK_L	63 64	FUNC_TEST=YES	
	UATA_DA<2..0>	6 63 64	FUNC_TEST=YES	
	UATA_CS0_L	6 63 64	FUNC_TEST=YES	
	UATA_CS1_L	63 64	FUNC_TEST=YES	
	UATA_RESET_L	63 64	FUNC_TEST=YES	
	UATA_HSTROBE	63 64	FUNC_TEST=YES	
	UATA_STOP	63 64	FUNC_TEST=YES	
	UATA_INTRO	63 64	FUNC_TEST=YES	
AUDIO	PP5V PWRON AUDIO PVDD	74	FUNC_TEST=YES	Place within 25 mm of audio connector.
	PP5V PWRON AUDIO AVDD	74	FUNC_TEST=YES	
	PP3V3 PWRON AUDIO AVDD	74	FUNC_TEST=YES	
	=PP3V3 RUN AUDIO	10 74	FUNC_TEST=YES	
	=I2C AUDIO_SCL	8 74	FUNC_TEST=YES	
	=I2C AUDIO_SDA	8 74	FUNC_TEST=YES	
	I2S0_MCLK	6 74	FUNC_TEST=YES	
	I2S0_BITCLK	6 74	FUNC_TEST=YES	
	I2S0_SYNC	6 74	FUNC_TEST=YES	
	I2S0_SB_TO_DEV DTO	6 74	FUNC_TEST=YES	
	I2S0_DEV_TO_SB DTI	22 74	FUNC_TEST=YES	
	AUDIO_LO MUTE_L	22 74	FUNC_TEST=YES	
	AUDIO_SPKR MUTE_L	22 74	FUNC_TEST=YES	
	AUDIO_CODEC RESET_L	22 74	FUNC_TEST=YES	
	AUDIO_SPDIFRX RESET_L	22 74	FUNC_TEST=YES	
	AUDIO_LO_DET_L	22 74	FUNC_TEST=YES	
	AUDIO_LI_DET_L	22 74	FUNC_TEST=YES	
	AUDIO_LO OPTICAL PLUG_L	22 74	FUNC_TEST=YES	
	AUDIO_LI OPTICAL PLUG_L	22 74	FUNC_TEST=YES	
	AUDIO_I2S DTIB_SEL	22 74	FUNC_TEST=YES	
	AUDIO_EXT MCLK_SEL	22 74	FUNC_TEST=YES	
	AUDIO_GPIO_11	22 74	FUNC_TEST=YES	
	GND AUDIO_AGND	74	FUNC_TEST=YES	
	GND AUDIO_PGND	74	FUNC_TEST=YES	

SYSTEM	PP5V_TPAD_F	30	FUNC_TEST=YES	Place within 25 mm of TPAD connector.
	USB_TPAD_P	11 30	FUNC_TEST=YES	
	USB_TPAD_N	11 30	FUNC_TEST=YES	
	PP3V3_PWRON_DS1775_R	30	FUNC_TEST=YES	
	SYS_OVERTEMP_L	11 25 30	FUNC_TEST=YES	
	PP3V3_ALL_HALL_EFFECT_R	30	FUNC_TEST=YES	
	SYS_LID_OPEN_F	30	FUNC_TEST=YES	
	SYS_POWER_BUTTON_L_F	30	FUNC_TEST=YES	
	=FTP_SLEEP_LED	30	FUNC_TEST=YES	
	SYS_CHARGE_LED_L	24 74	FUNC_TEST=YES	
	SYS_ADAPTER_ANALOG_AC_DET	12 74	FUNC_TEST=YES	
	KBDLED_ANODE	28 30	FUNC_TEST=YES	
	KBDLED_RETURN	28 30	FUNC_TEST=YES	
	=I2C_DS1775_SDA	8 30	FUNC_TEST=YES	
	=I2C_DS1775_SCL	8 30	FUNC_TEST=YES	
CPU FAN	=PP5V_FAN1_PWR	10 31	FUNC_TEST=YES	Place within 25 mm of fan connector.
	FAN1_TACH	27 31	FUNC_TEST=YES	
	FAN1_PWM	27 31	FUNC_TEST=YES	
	=FTP_GND	7 10	FUNC_TEST=YES	
GPU FAN	=PP5V_FAN2_PWR	10 31	FUNC_TEST=YES	Place within 25 mm of fan connector.
	FAN2_TACH	27 31	FUNC_TEST=YES	
	FAN2_PWM	27 31	FUNC_TEST=YES	
	=FTP_GND	7 10	FUNC_TEST=YES	
ALS	=PP3V3_PWRON_LEFT_ALS	10 31	FUNC_TEST=YES	Place within 25 mm of ALS connector.
	ALS_0_OUT	25 31	FUNC_TEST=YES	
	ALS_GAIN_BOOST	25 28 31	FUNC_TEST=YES	
SCCA	SCCA_RXD	22 24	FUNC_TEST=YES	Place within 25 mm of debug connector.
	SCCA_TXD_L	22 24	FUNC_TEST=YES	
BACKUP BATT	=PPVIO_BU_BATT	10 31	FUNC_TEST=YES	Place within 25 mm of battery connector.
	=PPVOUT_BU_BATT	10 31	FUNC_TEST=YES	
RT USB	=PP5V_PWRON_RIGHT_USB	10 31	FUNC_TEST=YES	Place within 25 mm of right USB connector.
	USB2_RIGHT_PORT_P	11 31	FUNC_TEST=YES	
	USB2_RIGHT_PORT_N	11 31	FUNC_TEST=YES	
LT USB	=PP5V_PWRON_LEFT_USB	10 74	FUNC_TEST=YES	Place within 25 mm of left USB connector.
	USB2_LEFT_PORT_P	11 74	FUNC_TEST=YES	
	USB2_LEFT_PORT_N	11 74	FUNC_TEST=YES	

Functional Test Points

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	D	DRAWING NUMBER	051-6929	REV.	03
SCALE	NONE	SHT	7	OF	115

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		DIFFERENTIAL_PAIR
		SPACING	PHYSICAL	
		I2C	I2C	I2C PMU SMB_SCL
		I2C	I2C	I2C PMU SMB_SDA
		I2C	I2C	I2C PMU_SCL
		I2C	I2C	I2C PMU_SDA
	I2C_NB	I2C	I2C	I2C I2_NB_SCL
	I2C_NB	I2C	I2C	I2C I2_NB_SDA
		I2C	I2C	I2C I2_SB_SCL
		I2C	I2C	I2C I2_SB_SDA
		I2C	I2C	I2C GPU_TMDS_SCL
		I2C	I2C	I2C GPU_TMDS_SDA

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

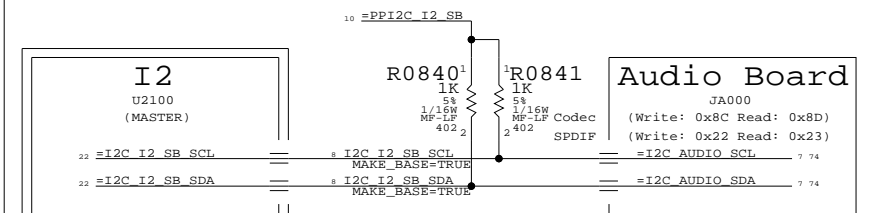
BOM options provided by this page:
- GOV_I2C / GOV_I2C_BYPASS

Allows bypassing Governor I2C bus.
Most devices are connected directly to
PMU instead. One ADT7467 connects to NB
I2C bus 1 to resolve address conflict.

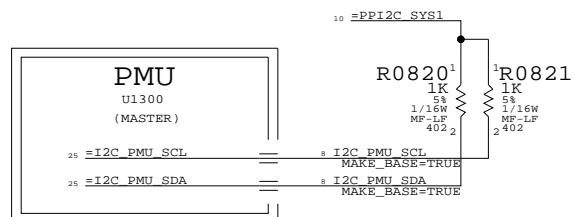
- MMM_PWR_ALL / MMM_PWR_PWRON

Selects whether MMM MCU is powered all the time or only when the system is on. ALL moves the MCU to the PMU I2C bus so it can be monitored by in shutdown.

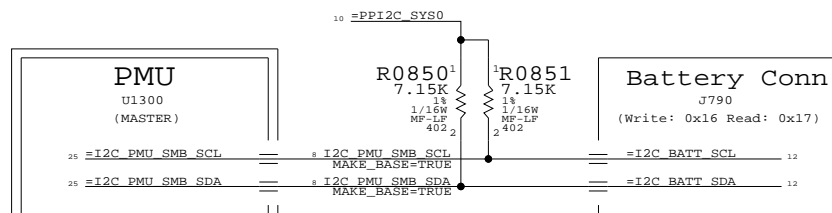
NOTE: Neither option is necessary when MMM_MCU_PMU BOM option is selected.



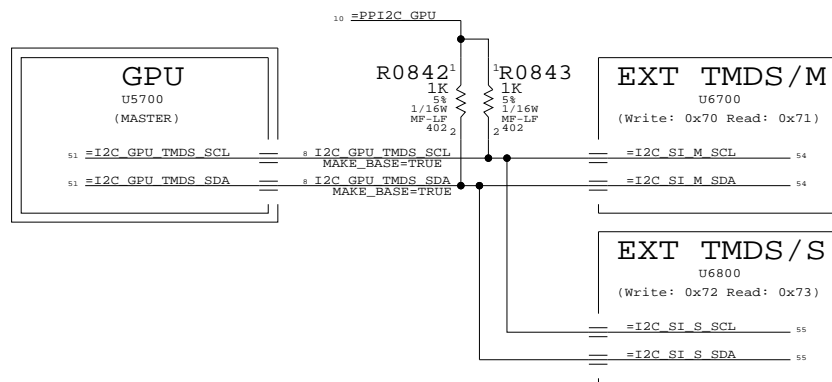
PMU I2C Bus



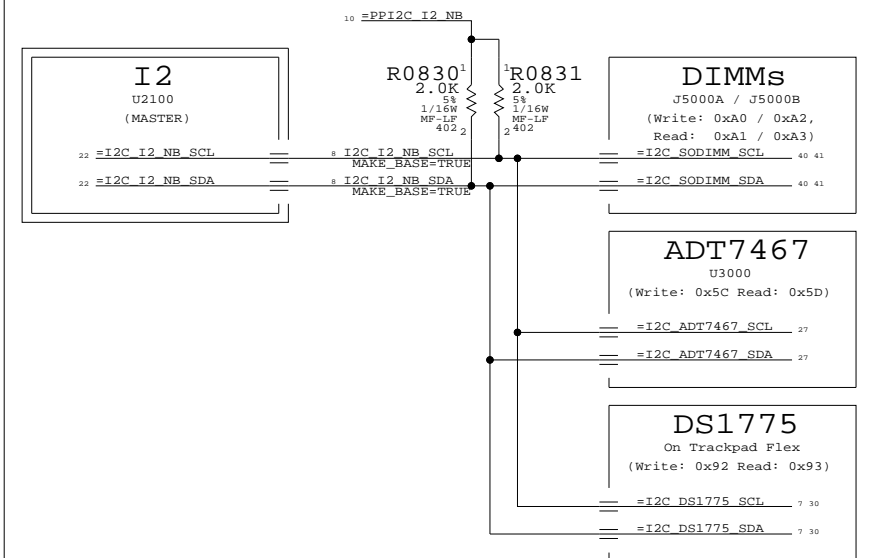
PMU SMBus



GPU I2C Bus



NorthBridge I2C Bus



I2C Connections

SYNC_MASTER=N/A	SYNC_DATE=N/A
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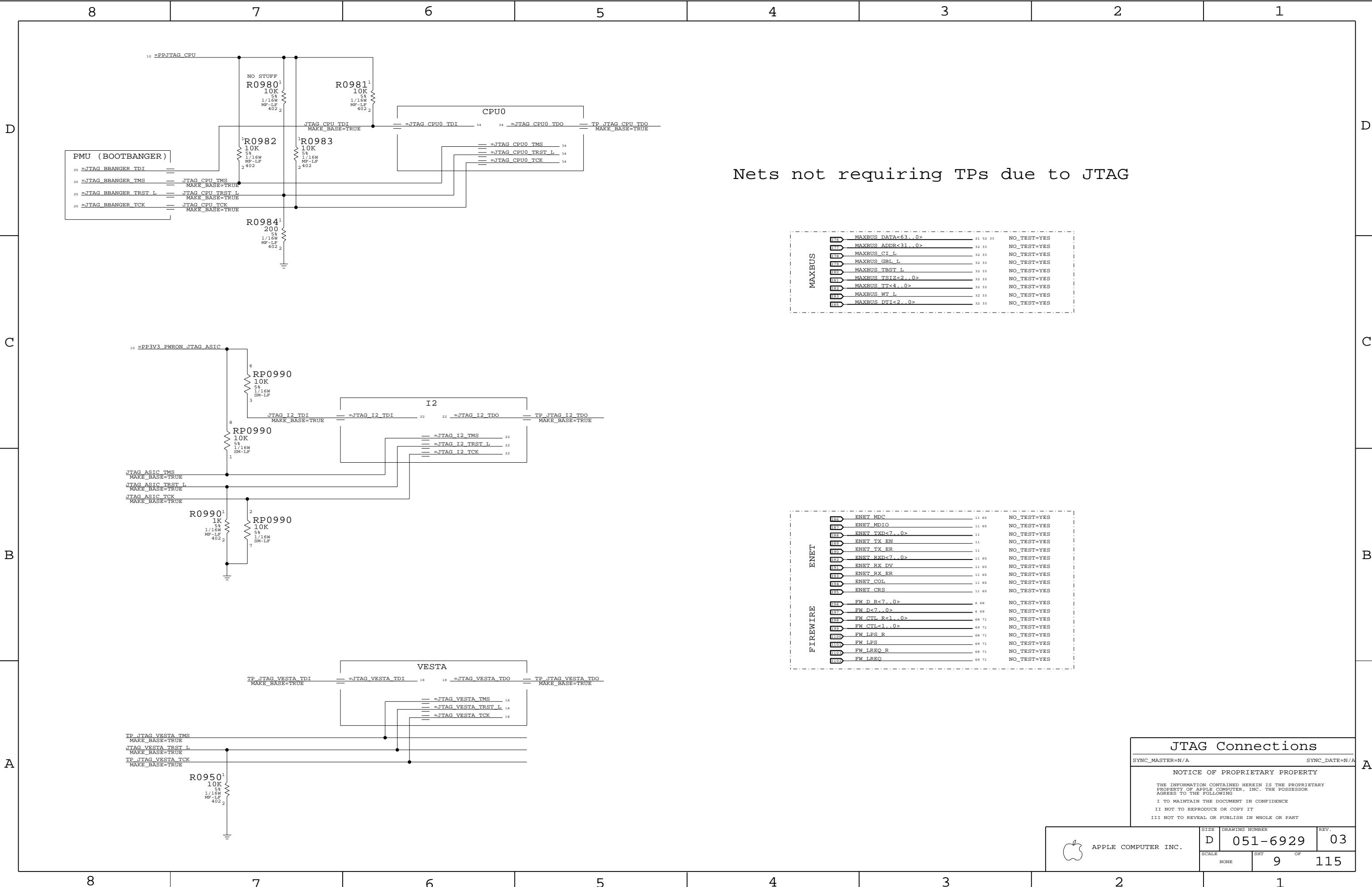


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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D	051-6929	03
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SCALE	SHT	OF
NONE	8	115



Nets not requiring TPs due to JTAG

MAXBUS	MAXBUS_DATA<63..0>	21 32 33	NO_TEST=YES
	MAXBUS_ADDR<31..0>	32 33	NO_TEST=YES
	MAXBUS_CI_L	32 33	NO_TEST=YES
	MAXBUS_GBL_L	32 33	NO_TEST=YES
	MAXBUS_TBST_L	32 33	NO_TEST=YES
	MAXBUS_TSIz<2..0>	32 33	NO_TEST=YES
	MAXBUS_TT<4..0>	32 33	NO_TEST=YES
	MAXBUS_WT_L	32 33	NO_TEST=YES
MAXBUS	MAXBUS_DTI<2..0>	32 33	NO_TEST=YES

ENET	ENET_MDC	11 65	NO_TEST=YES
	ENET_MDIO	11 65	NO_TEST=YES
	ENET_TXD<7..0>	11	NO_TEST=YES
	ENET_TX_EN	11	NO_TEST=YES
	ENET_TX_ER	11	NO_TEST=YES
	ENET_RXD<7..0>	11 65	NO_TEST=YES
	ENET_RX_DV	11 65	NO_TEST=YES
	ENET_RX_ER	11 65	NO_TEST=YES
FIREWIRE	ENET_COL	11 65	NO_TEST=YES
	ENET_CRS	11 65	NO_TEST=YES
	FW_D_R<7..0>	6 68	NO_TEST=YES
	FW_D<7..0>	6 69	NO_TEST=YES
	FW_CTL_R<1..0>	68 71	NO_TEST=YES
	FW_CTL<1..0>	69 71	NO_TEST=YES
	FW_LPS_R	68 71	NO_TEST=YES
	FW_LPS	69 71	NO_TEST=YES
FIREWIRE	FW_LREQ_R	68 71	NO_TEST=YES
	FW_LREQ	69 71	NO_TEST=YES

JTAG Connections

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SHT	OF
NONE	9	115



Power Synonyms	
SYNC_MASTER=N/A	SYNC_DATE=N/A
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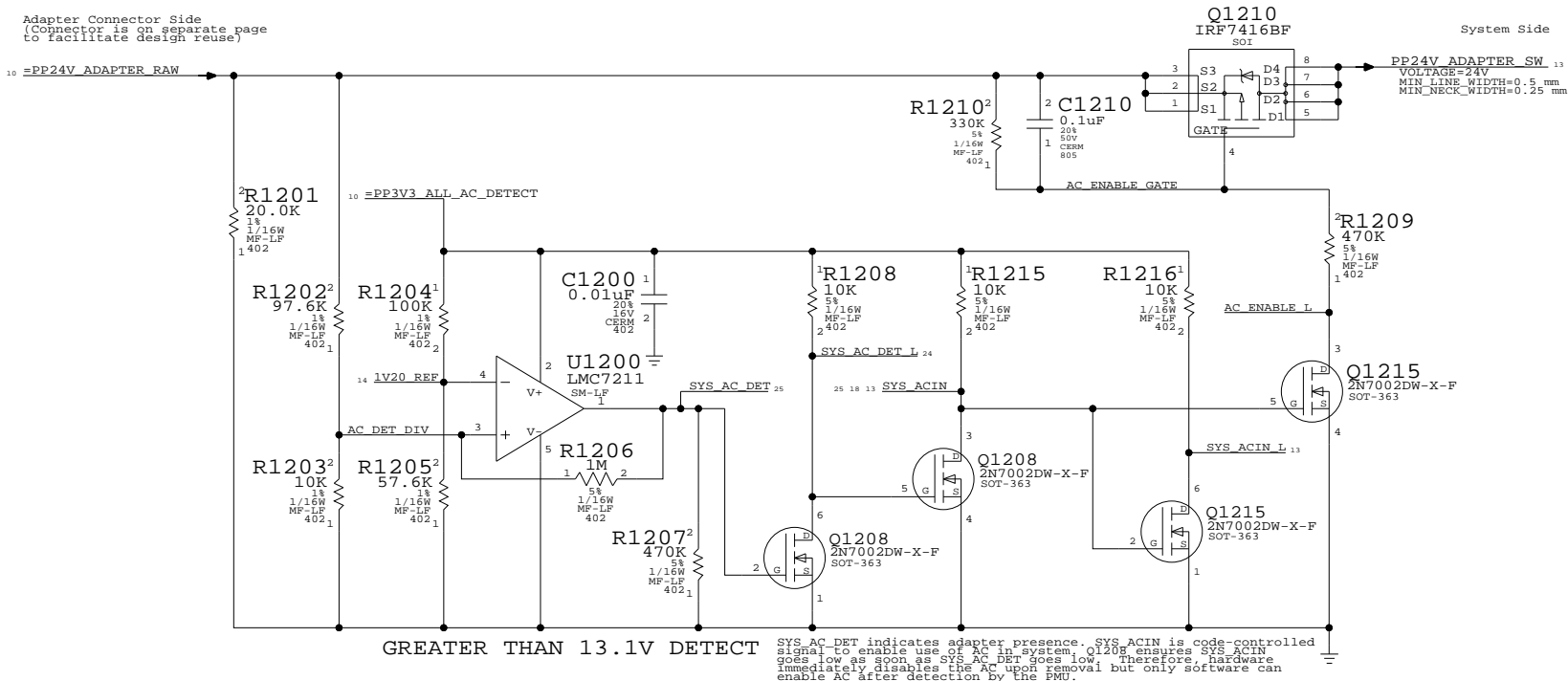
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	SIT		OF
	NONE		10 115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
B310		THERM	THERM
B310		THERM	THERM

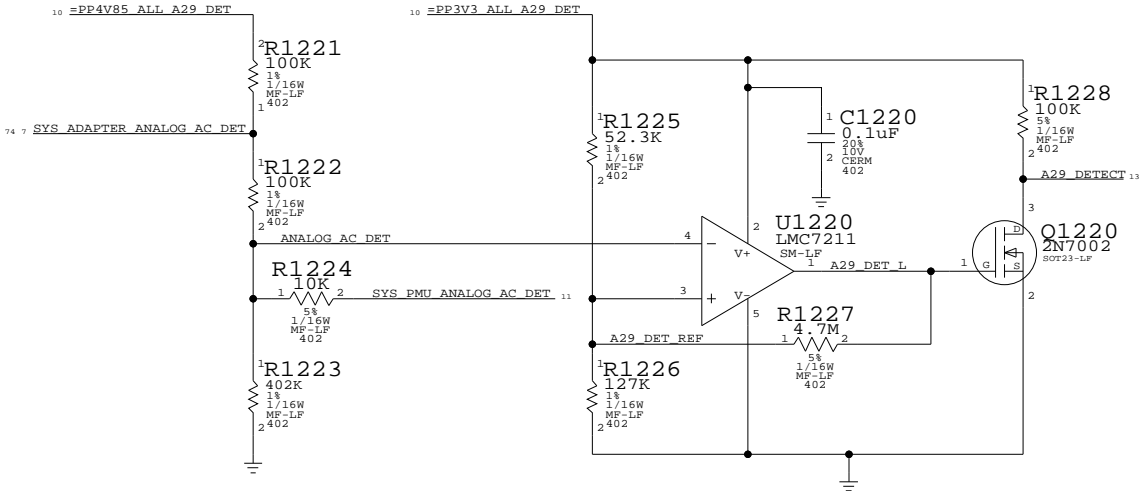
PPVBATT ISNS VINP	12
PPVBATT ISNS VINN	12

ADAPTER INPUT/INRUSH LIMITER

Adapter Connector Side
(Connector is on separate page
to facilitate design reuse)

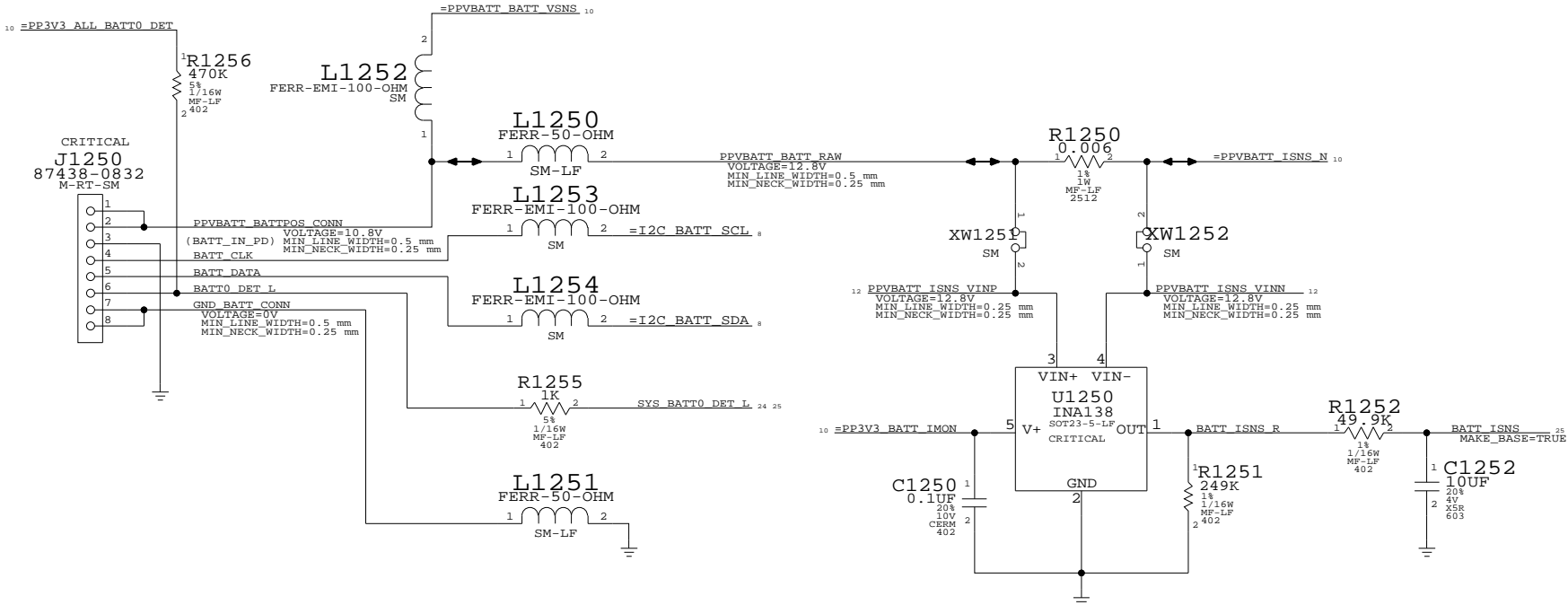


A29 ADAPTER DETECTION



ADAPTER IDS		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V

BATTERY INPUT/CURRENT SENSE



Power Inputs

SYNC_MASTER=N/A SYNC_DATE=N/A

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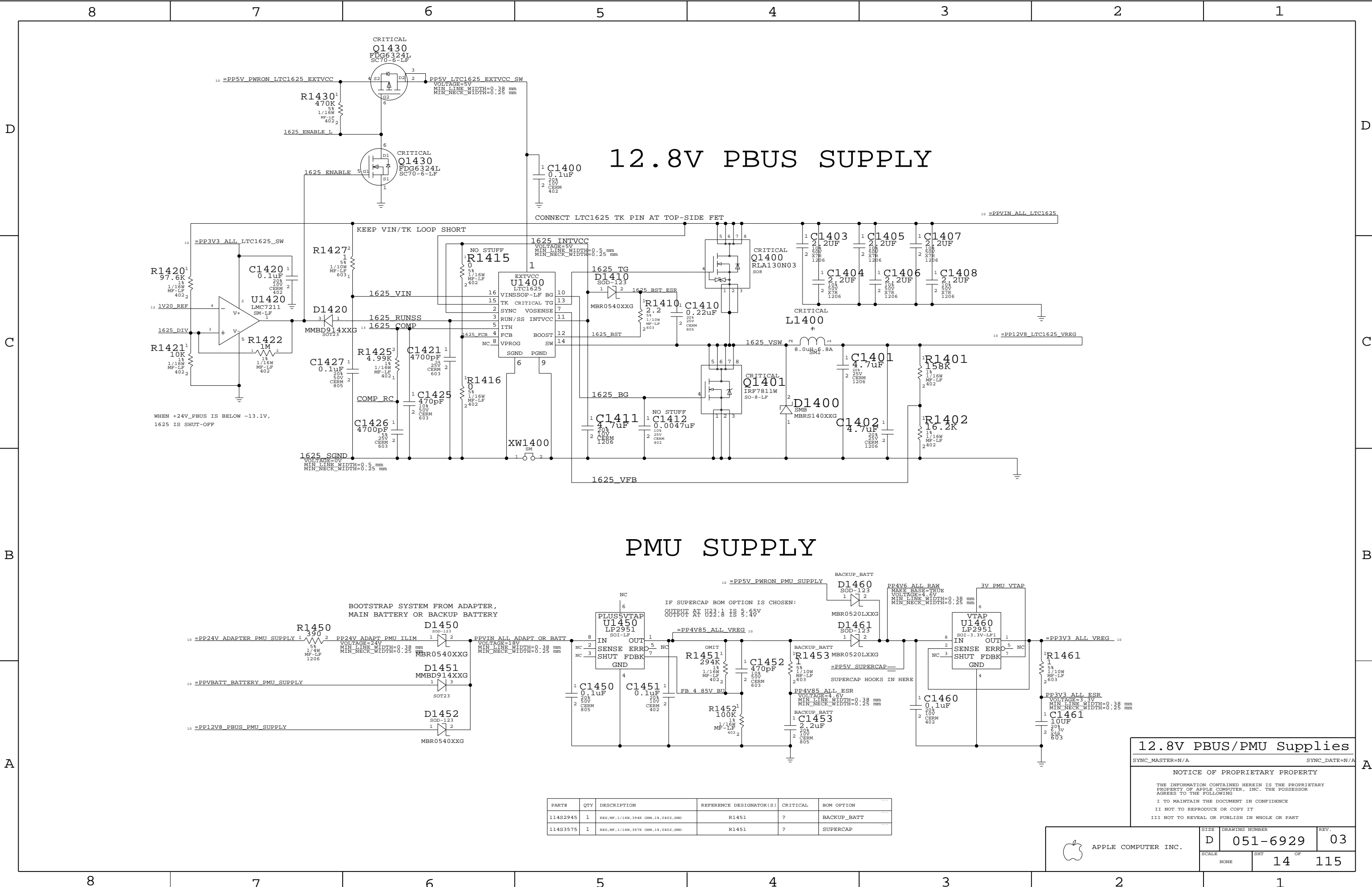
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	12	115



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2945	1	RES,MP,1/16W,394K OHM,1%,0402,SMD	R1451	?	BACKUP_BATT
114S3575	1	RES,MP,1/16W,357K OHM,1%,0402,SMD	R1451	?	SUPERCAP

12.8V PBUS/PMU Supplies

SYNC_MASTER=N/A SYNC_DATE=N/A

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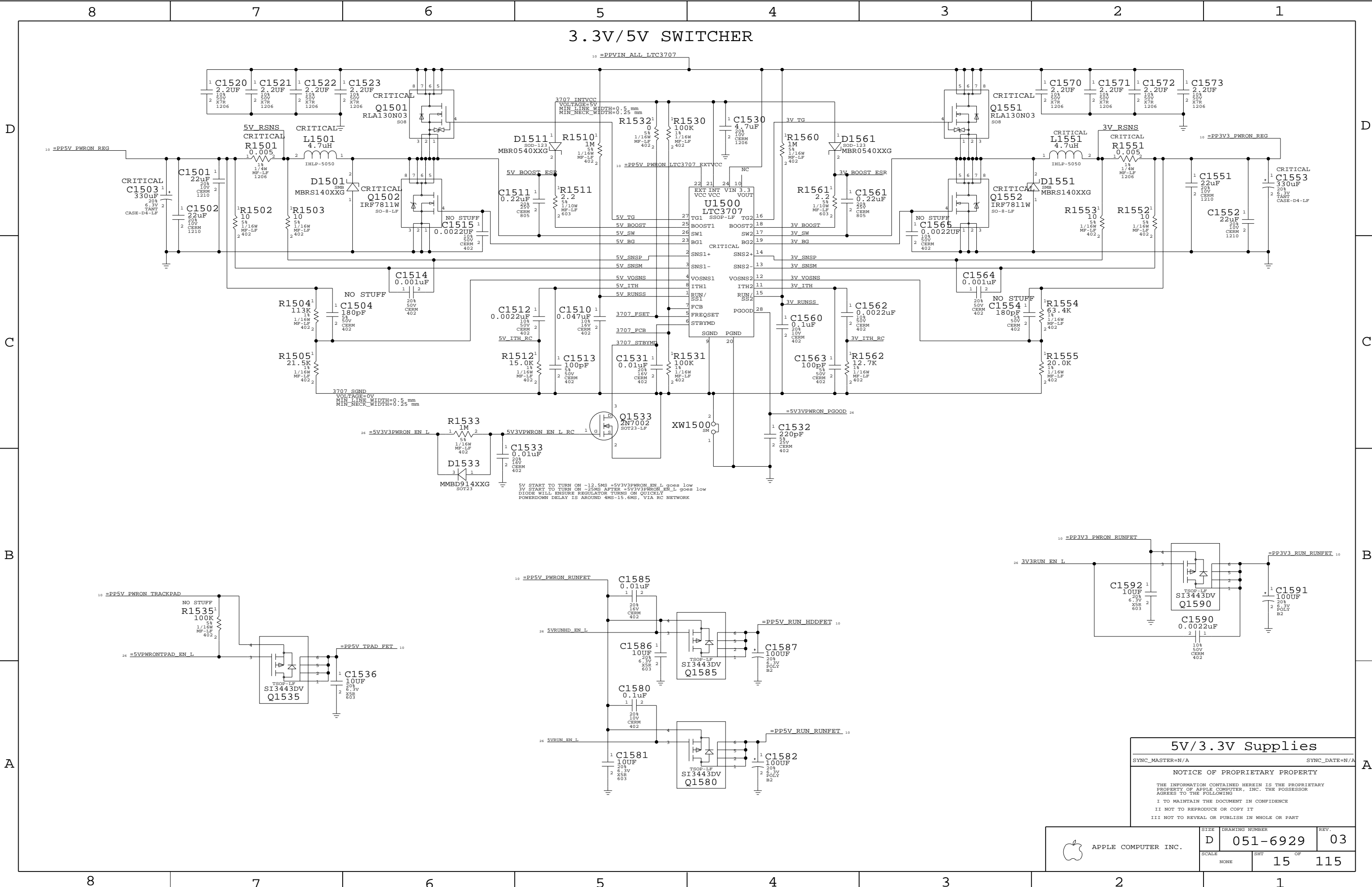
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	14	115



5V/3.3V Supplies

SYNC_MASTER=N/A SYNC_DATE=N/A

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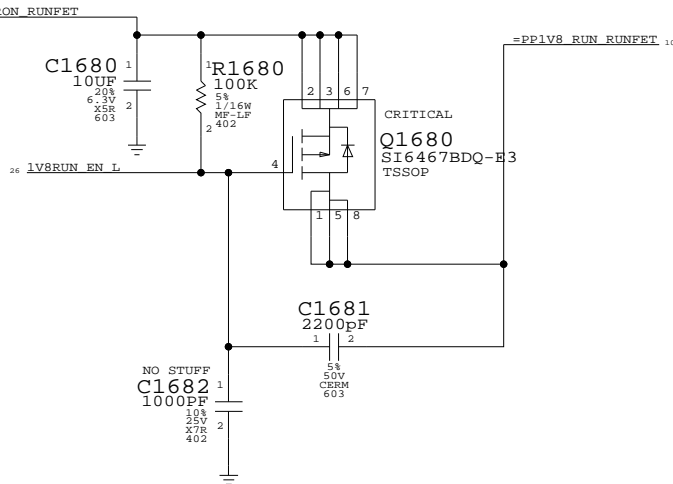
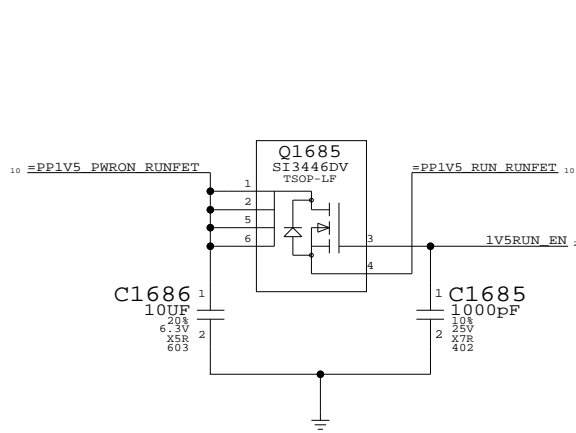
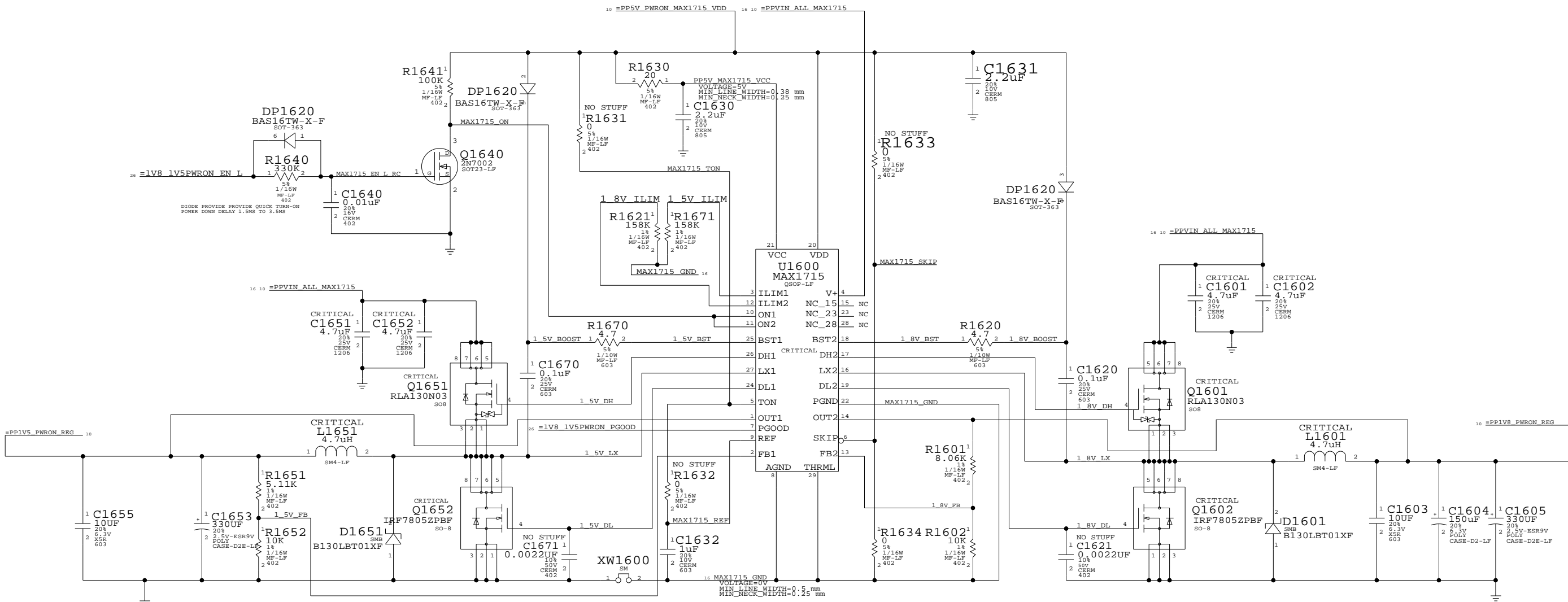
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	D	051-6929	03
	SCALE	SHT	OF
	NONE	15	115

1.5V/1.8V SWITCHER



1.8V/1.5V Supplies

SYNC_MASTER=N/A SYNC_DATE=N/A

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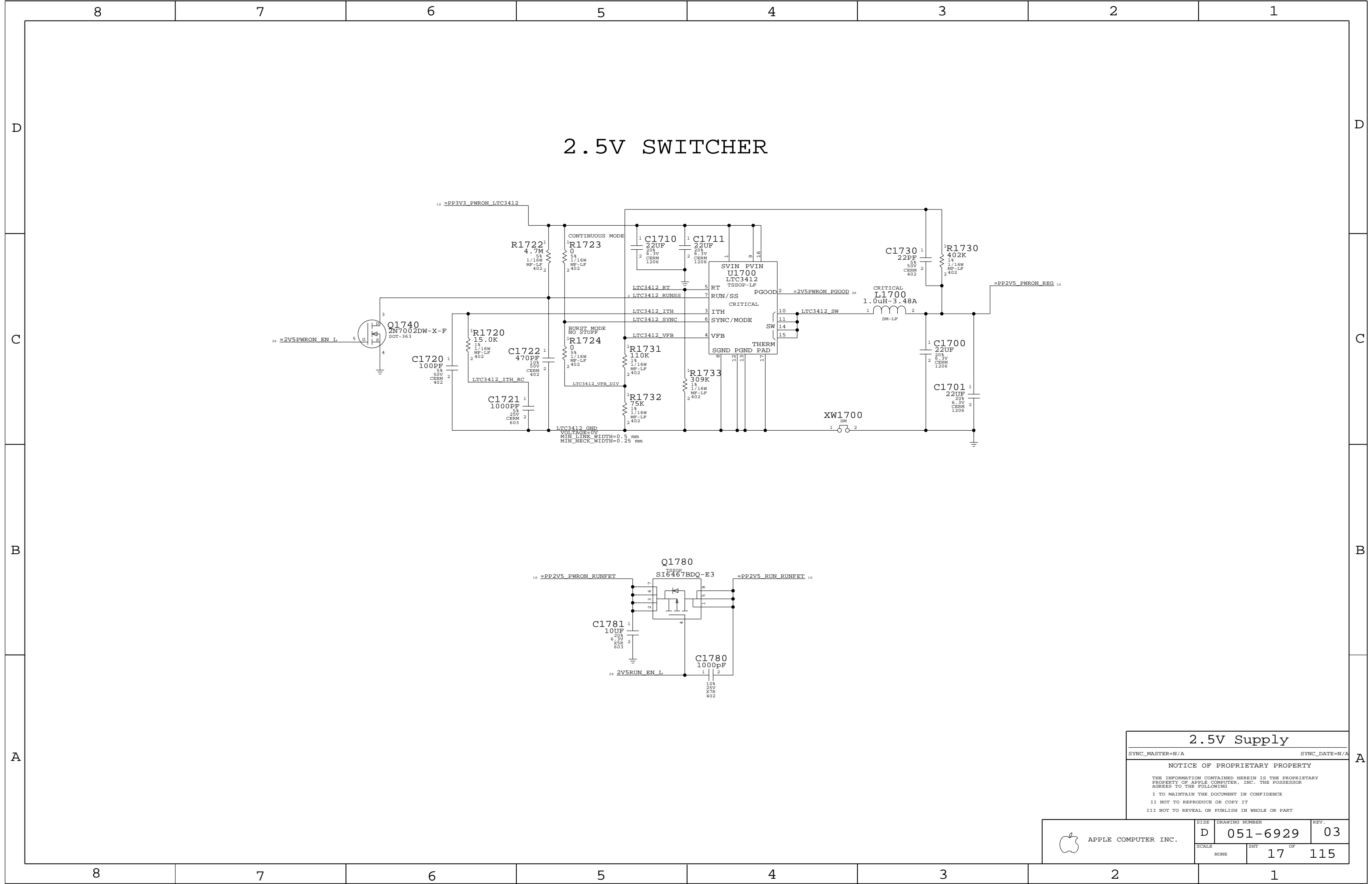
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	16	115



2.5V Supply

SYNC_MASTER=N/A

SYNC_DATE=N/A

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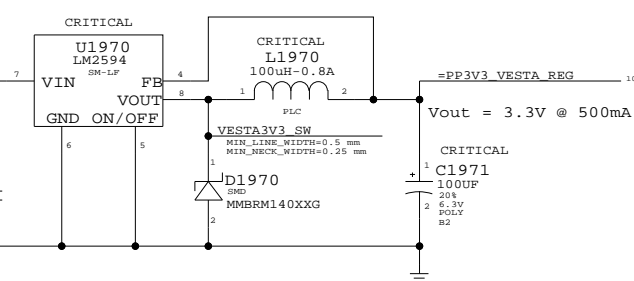
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE		SHT	OF
NONE		17	115

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

D



CRITICAL

U1980

MM1572FN

SOT-25A

REG

VIN

VOUT

CONT

NOISE

GND

VESTA2V5 NOISE

MIN_LINE_WIDTH=0.2 mm

MIN_NECK_WIDTH=0.2 mm

C1980

1uF

10V

6.3V

CERN

402

C1981

0.01uF

20V

16V

CERN

402

C1982

10UF

20V

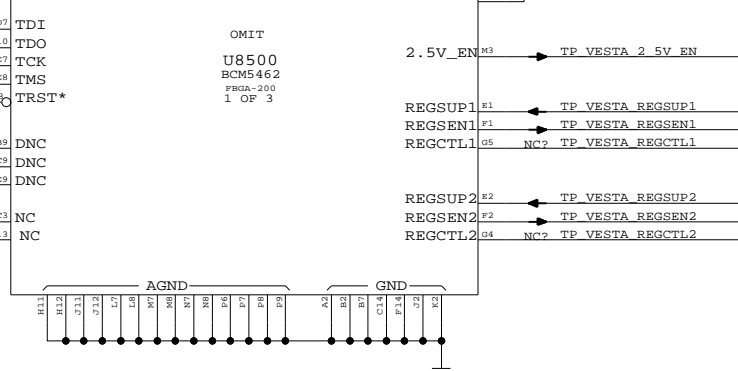
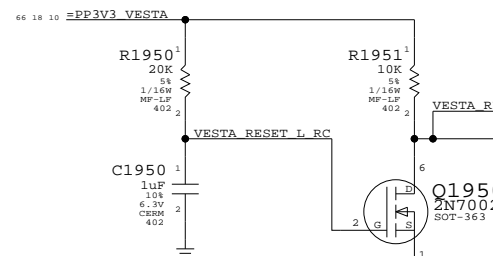
6.3V


25R

603

=PEZV5 VESTA LDO

Vout = 2.5V @ 150 mA

[illegible]

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
	SCALE	SHT	OF
	NONE	19	115



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER
------	----------------

COMPUTER INC.

	SHT
--	-----

	REV
--	-----

03

115

8

7

6

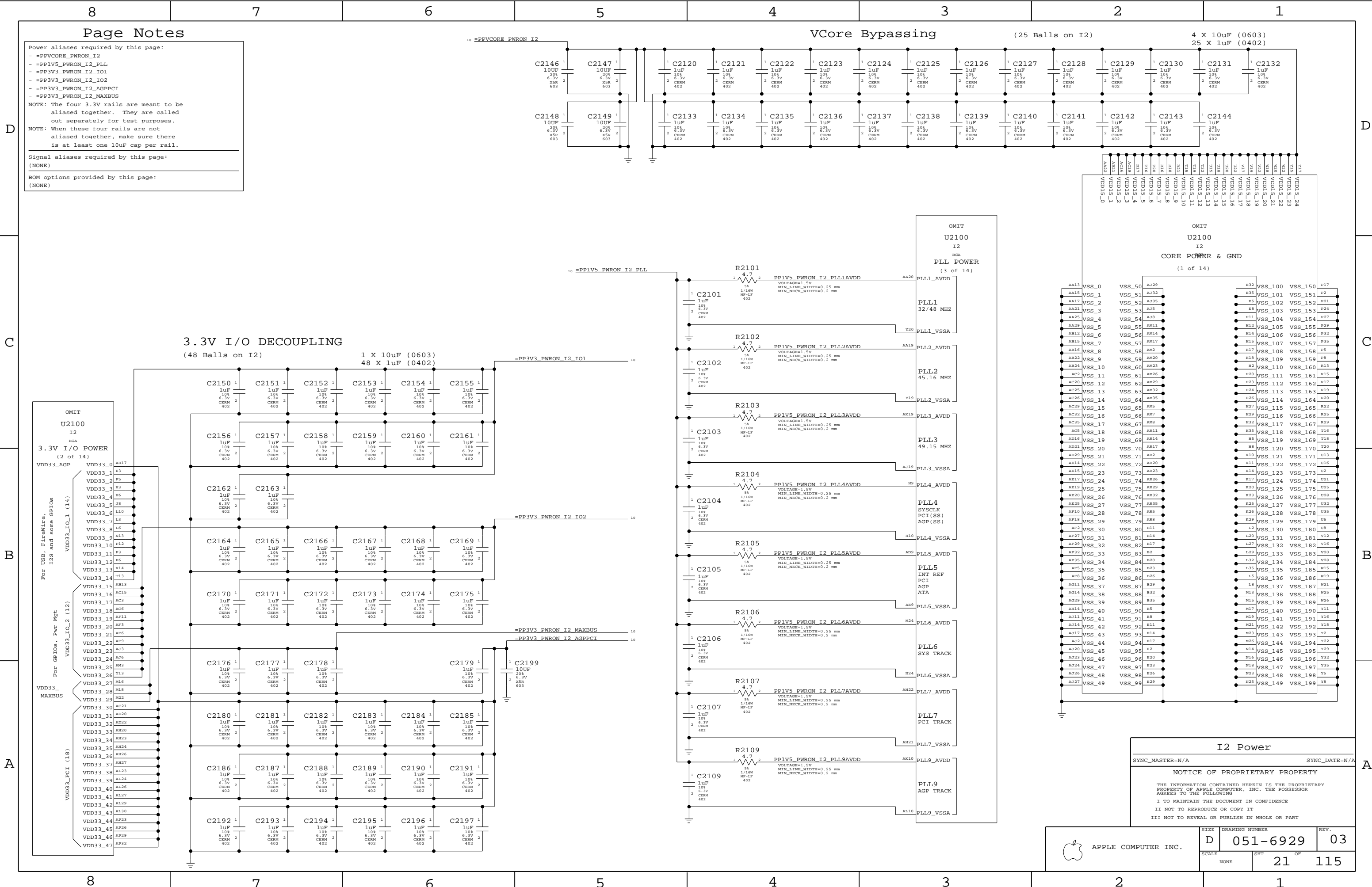
5

4

3

2

1



Page Notes

Power aliases required by this page:

- =PPVCORE_PWRON_I2
- =PP1V5_PWRON_I2_PLL
- =PP3V3_PWRON_I2_IO1
- =PP3V3_PWRON_I2_IO2
- =PP3V3_PWRON_I2_AGPPCI
- =PP3V3_PWRON_I2_MAXBUS

NOTE: The four 3.3V rails are meant to be aliased together. They are called out separately for test purposes.

NOTE: When these four rails are not aliased together, make sure there is at least one 10uF cap per rail.

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

3.3V I/O DECOUPLING
(48 Balls on I2)

1 X 10uF (0603)
48 X 1uF (0402)

VCore Bypassing

(25 Balls on I2)

4 X 10uF (0603)
25 X 1uF (0402)

I2 Power

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	21	115

Power aliases required by this page:

- =PP2V7R5V5_PWRON_I2VCORE
- =PPVCORE_PWRON_I2_REG
- =PPVIN_PWRON_I2PLLVD
- =PP1V5_PWRON_I2PLLVD_LDO

Signal aliases required by this page:

- =I2VCORE_PGOOD

BOM options provided by this page:

- I2VCORE_CONT / I2VCORE_BURST
Selects between forced continuous and burst mode for LTC3412 regulator.
- I2VCORE_xVx
Selects appropriate resistor for the indicated LTC3412 output voltage.

The schematic diagram illustrates the I2VCONV board layout. It features a central I2VCONV module with pins labeled SVIN PVIN, U2200, L2V3412, and T2V3412. The module is connected to various components including resistors (R2201-R2209), capacitors (C2201-C2216), and a switch (SW). The board is powered by a 5V supply (V5) and a 0.8V supply (V8). The output voltage (Vout) is determined by the ratio of resistors Rb1 and Rb2, as shown in the table below.

PART NUMBER	QTY	DESCRIPTION	REFERENCE
114S0437	1	RES,185K,1%,MF-LF,0402	R2201
114S0442	1	RES,210K,1%,MF-LF,0402	R2202
114S0446	1	RES,232K,1%,MF-LF,0402	R2203

One for each PVIN pin

Vout = 0.8V * (1 + (Ra / (Rb1 + Rb2)))

CRITICAL L2200 1.0uH-3.48A

Open-Collector

PFVCONV_PWRON_I2VCONV

GND I2VCONV

Voltage=0V

MIN_LINE_WIDTH=0.75 mm

MIN_NECK_WIDTH=0.25 mm

I2VCONV_MODE_VDIV

If I2VCONV_BURST is selected:

Iburst = (Vburst - 0.2V) * (3.75A / 0.8V)

Vburst = 0.8V * (Rb2 / (Rb1 + Rb2))

The schematic diagram shows the PLL circuit for the AD9548. It includes a U2250 LT1962-ADJ voltage detector, a U2254 0.01uF capacitor, and a U2256 68.1K resistor. The output voltage is $V_{out} = 1.22V * (1 + R_a/R_b) + (I_{adj} * R_a)$. The current I_{adj} is 30nA at 25 C. The circuit is powered by PP1V5_PWRON_I2PLL_LDO and PPVIN_PWRON_I2PLL_VDD. The output is connected to the I2PLL_VDD pin of the AD9548.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0437	1	RES,185K,1%,MF-LF,0402	R2210		I2VCORE_1v6
114S0442	1	RES,210K,1%,MF-LF,0402	R2210		I2VCORE_1v7
114S0446	1	RES,232K,1%,MF-LF,0402	R2210		I2VCORE_1v8

I2 Power Supplies

SYNC_MASTER=N/A SYNC_DATE=N/A

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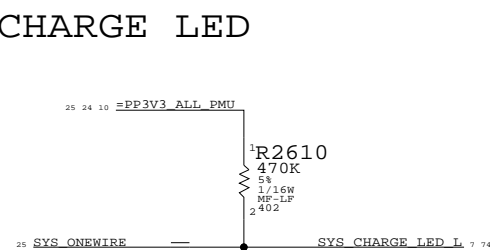
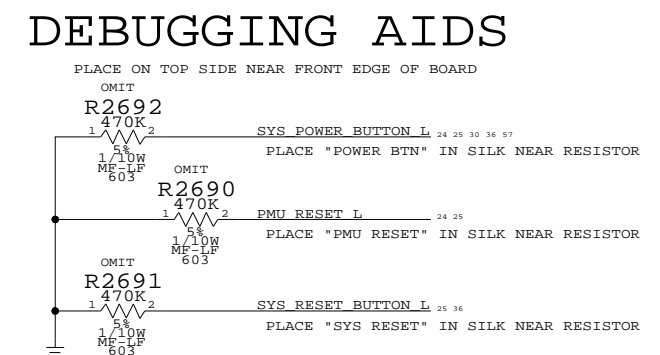
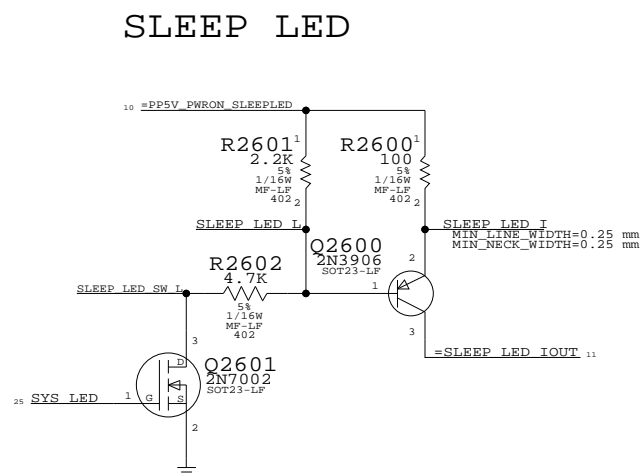
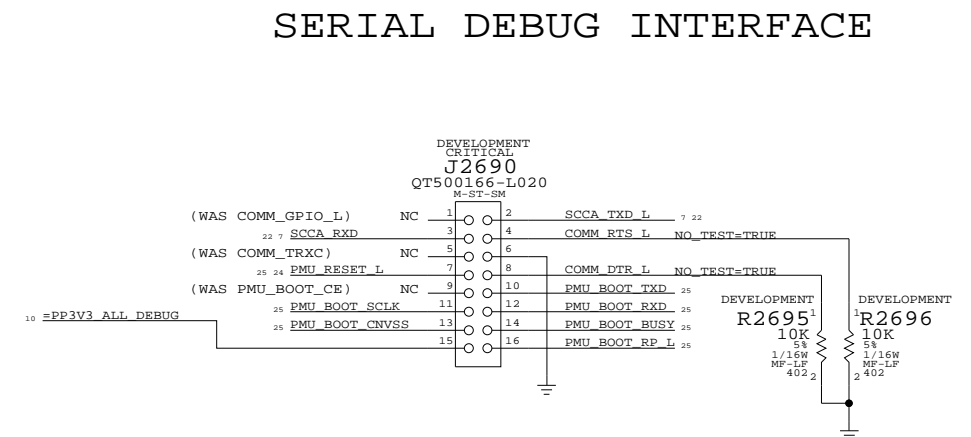
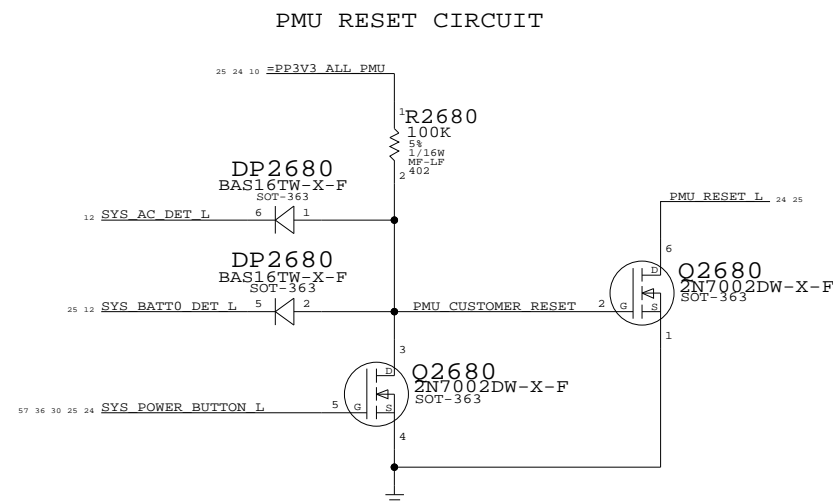
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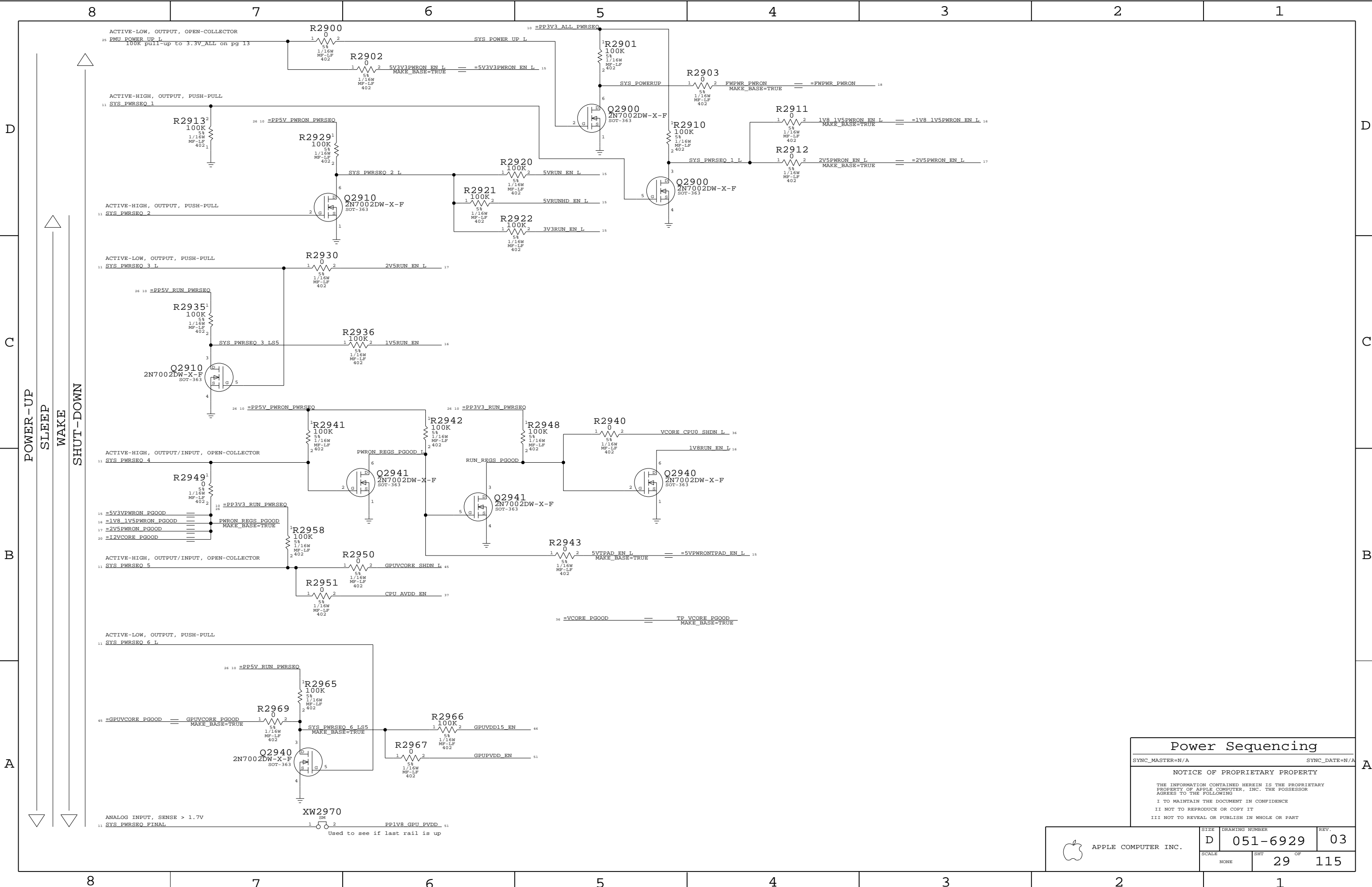
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SIZE	DRAWING NUMBER		REV.
D	051-6929		03
SCALE		SHT	OF
NONE		22	115



LEDs/Reset/Debug	
SYNC_MASTER=N/A	SYNC_DATE=N/A
A	
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	D	051-6929	03
	SCALE	SHT	
	NONE	26	115



Power Sequencing

SYNC_MASTER=N/A

SYNC_DATE=N/A

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	D	051-6929	03
SCALE	SHT		OF
	NONE	29	115

D

C

B

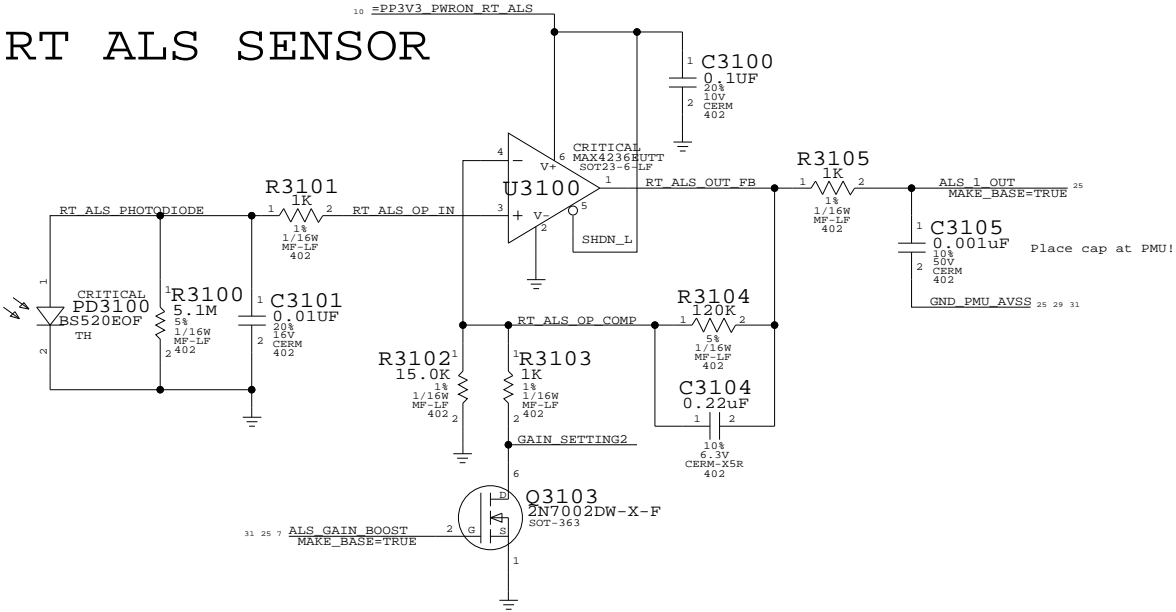
A

D

C

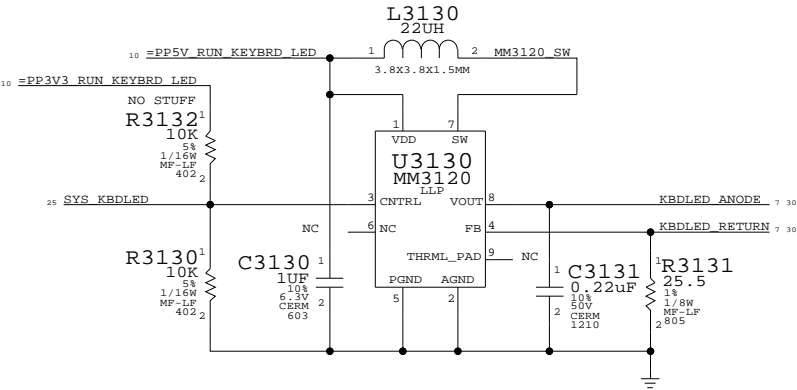
B

A



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U3100	

Keyboard LED Driver



ALS Support

SYNC_MASTER=N/A SYNC_DATE=N/A

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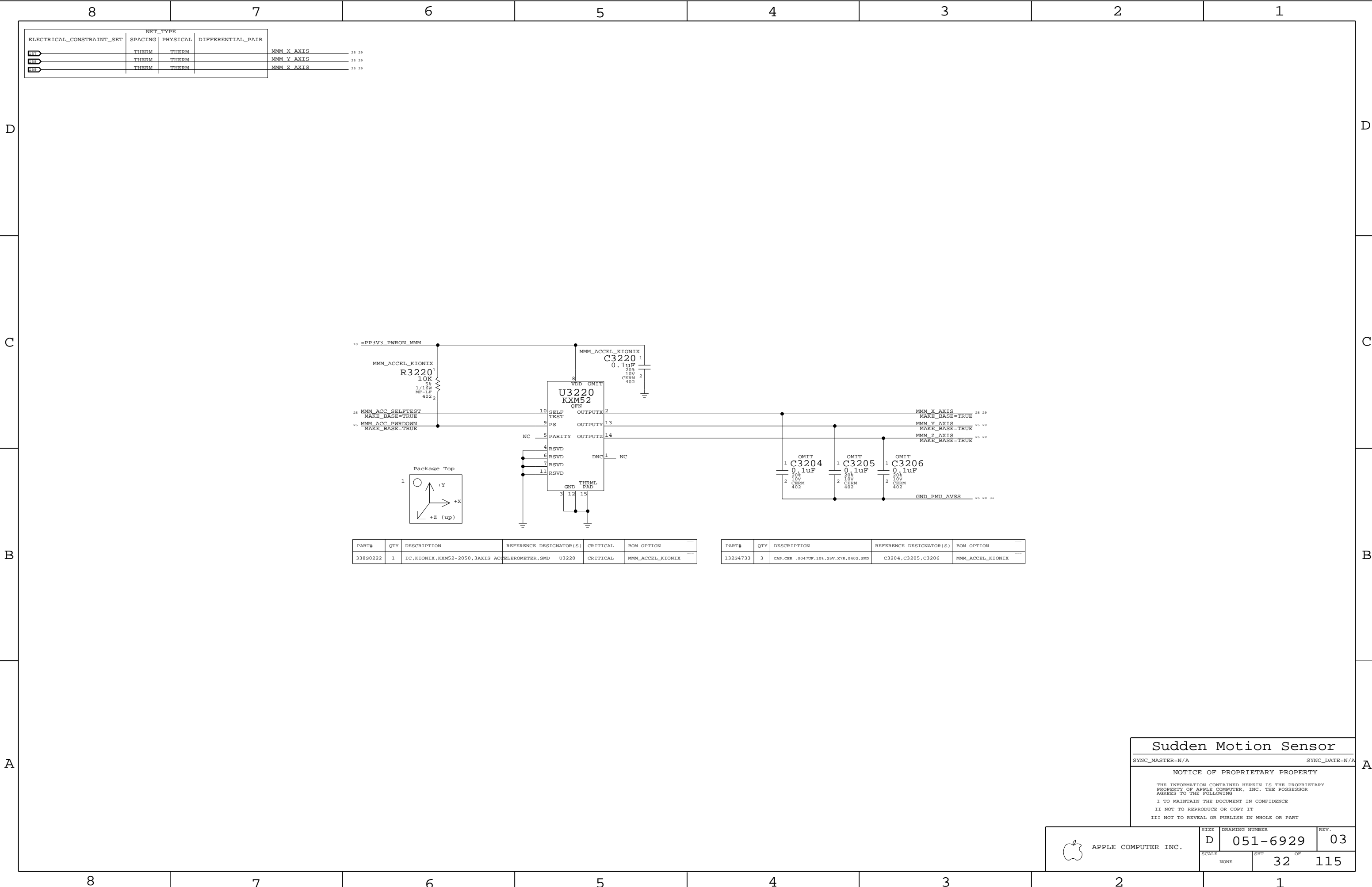
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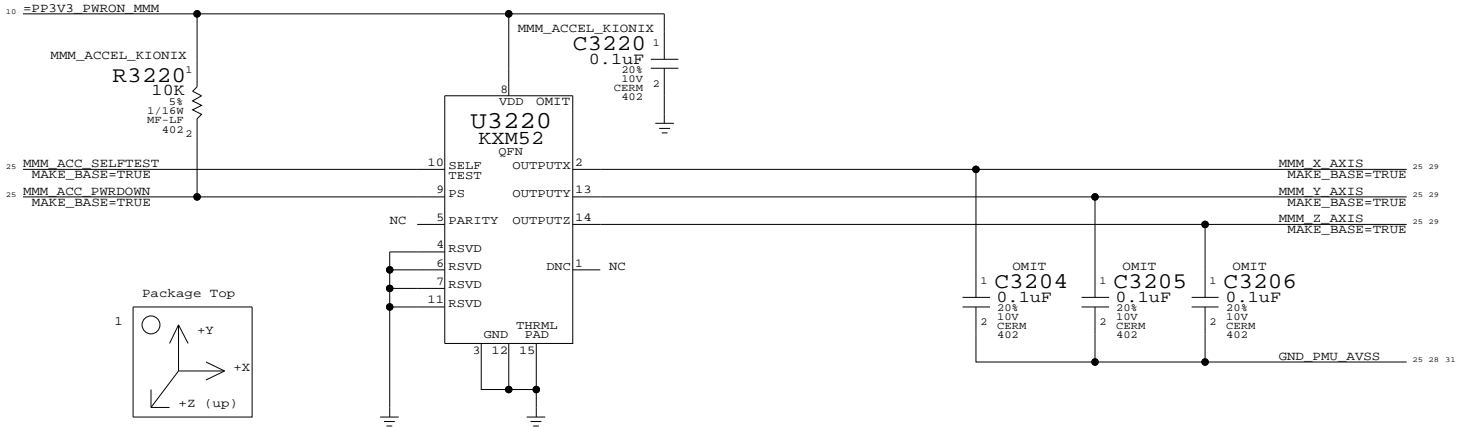
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SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	31	115



ELECTRICAL_CONSTRAINT_SET	NET_TYPE			DIFFERENTIAL_PAIR
	SPACING	PHYSICAL		
ES7		THERM	THERM	
ES8		THERM	THERM	
ES9		THERM	THERM	

MMM X AXIS	25	29
MMM Y AXIS	25	29
MMM Z AXIS	25	29



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0222	1	IC,KIONIX,KXM52-2050,3AXIS ACCELEROMETER,SMD	U3220	CRITICAL	MMM_ACCEL_KIONIX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S4733	3	CAP,CER .0047UF,10%,25V,X7R,0402,SMD	C3204,C3205,C3206	MMM_ACCEL_KIONIX

Sudden Motion Sensor

SYNC_MASTER=N/A SYNC_DATE=N/A

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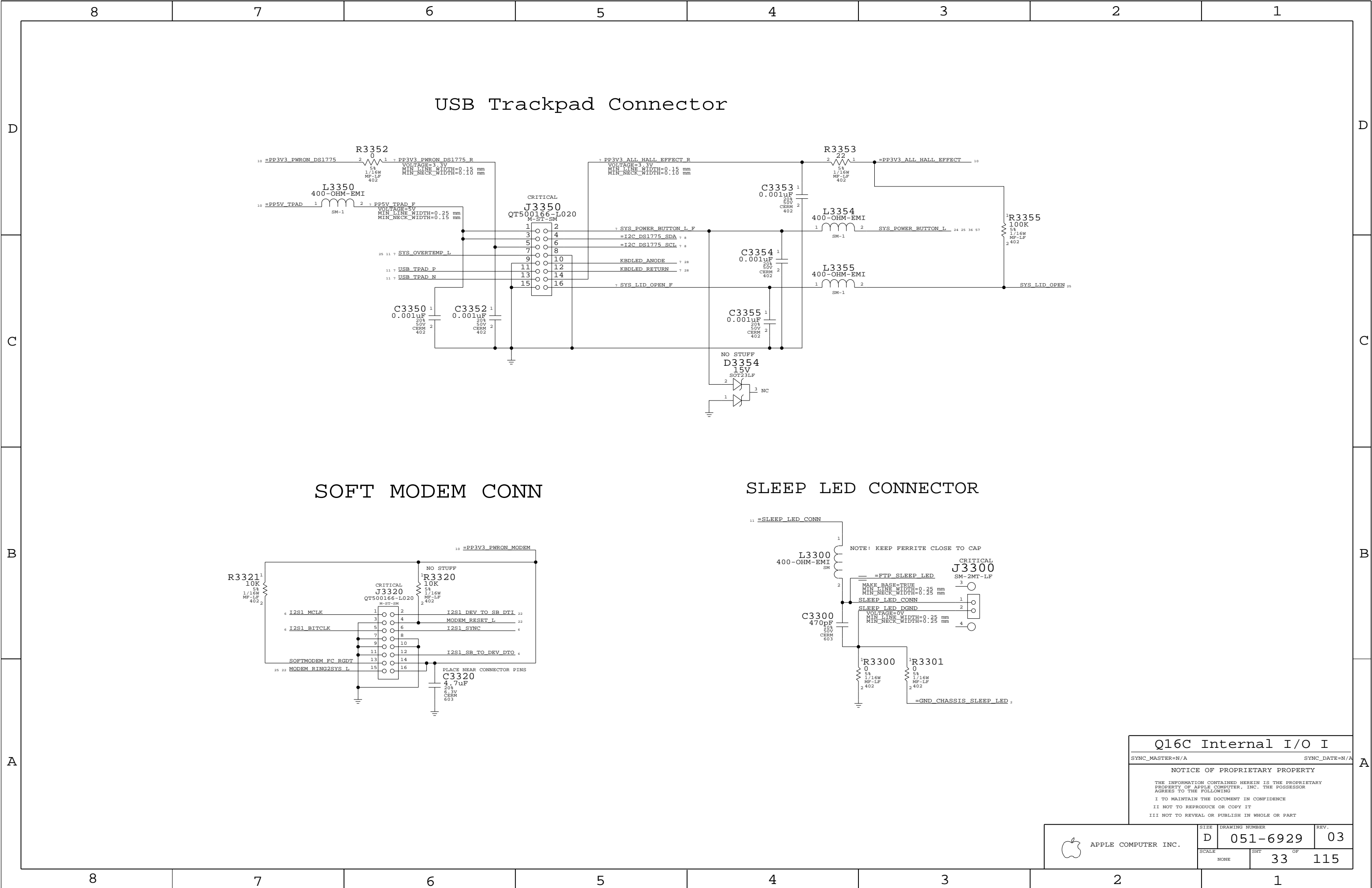
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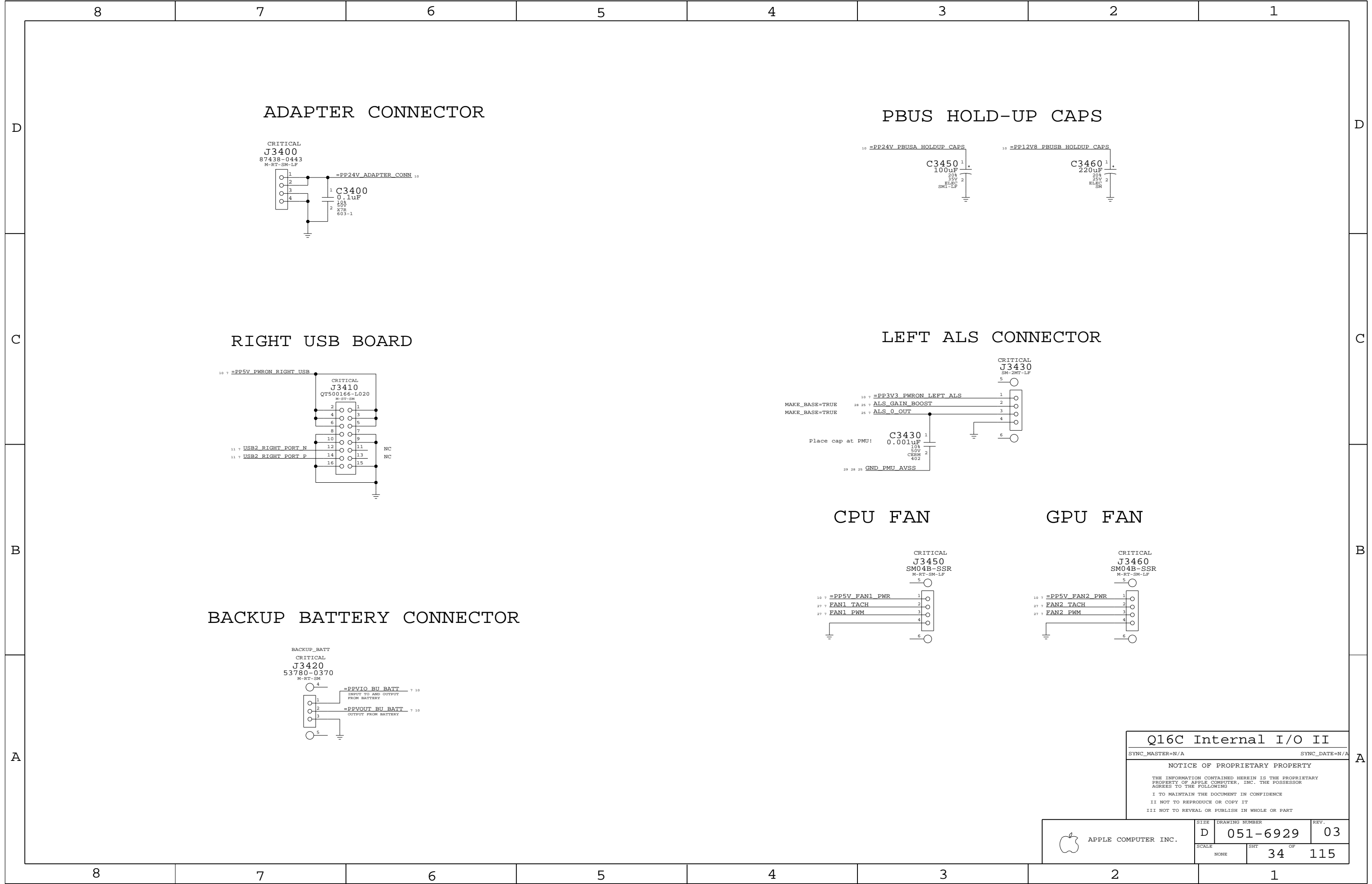
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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-6929 REV. 03

SCALE NONE SHT 32 OF 115





Q16C Internal I/O II

SYNC_MASTER=N/A SYNC_DATE=N/A

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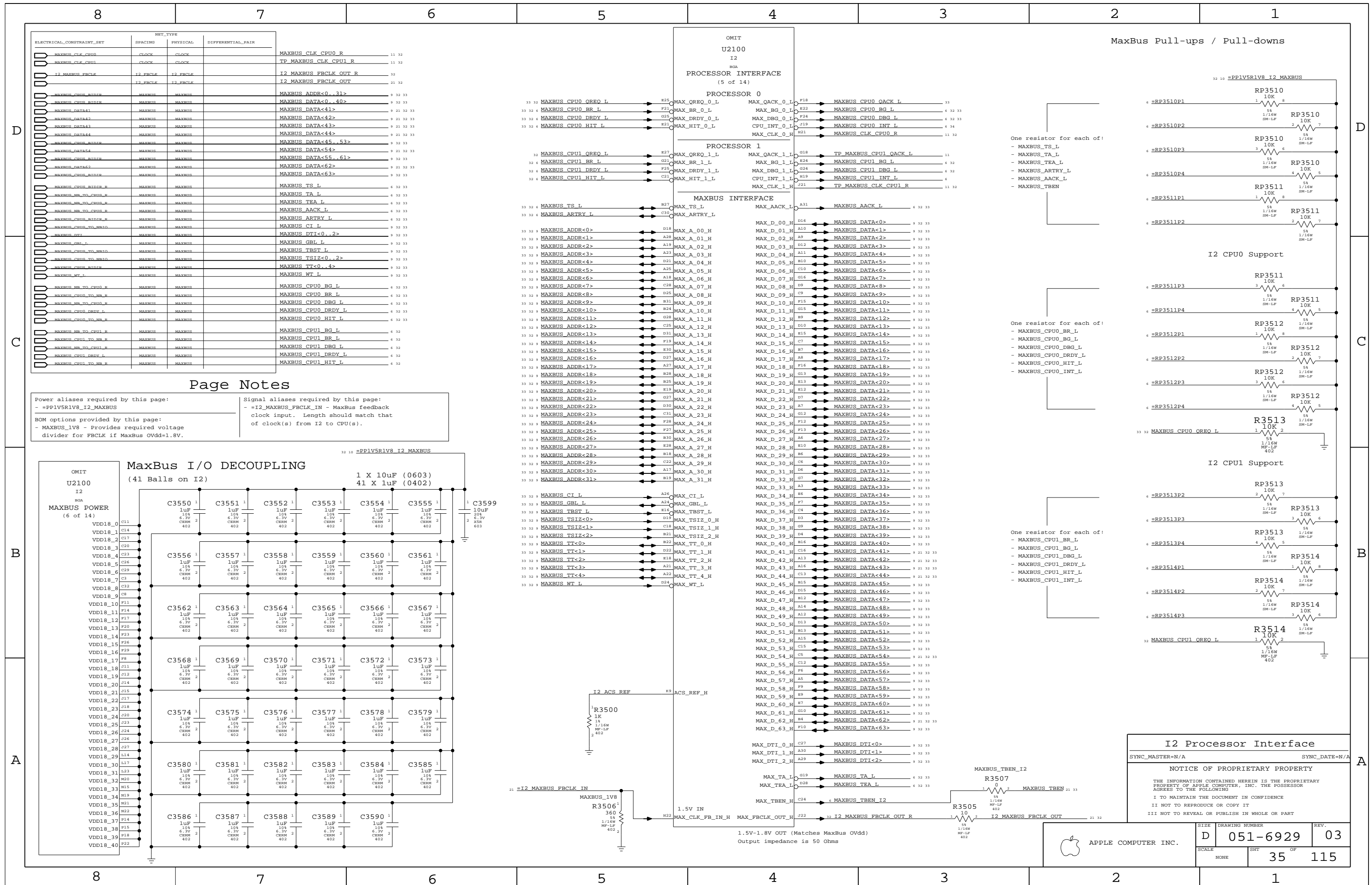
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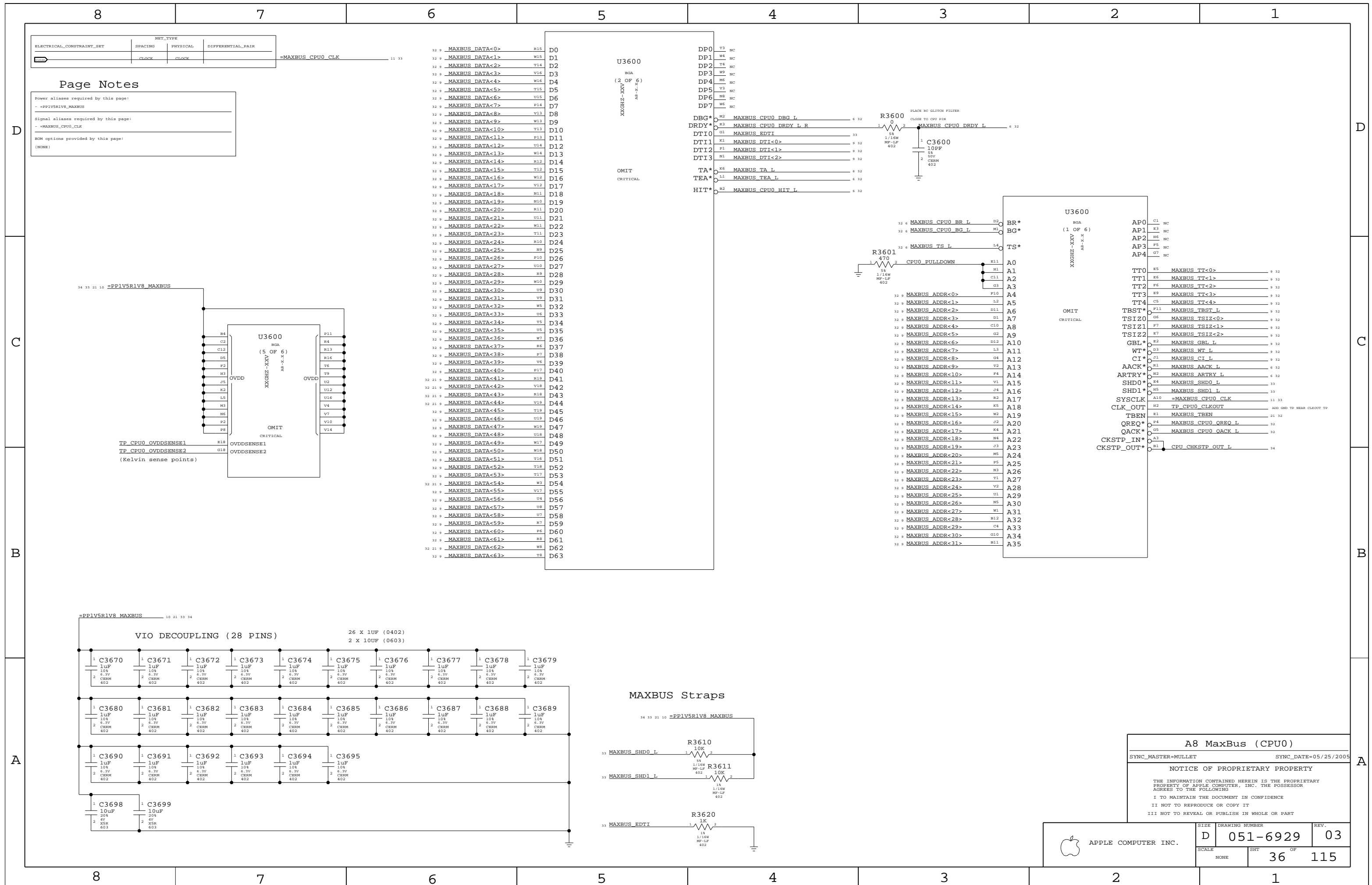
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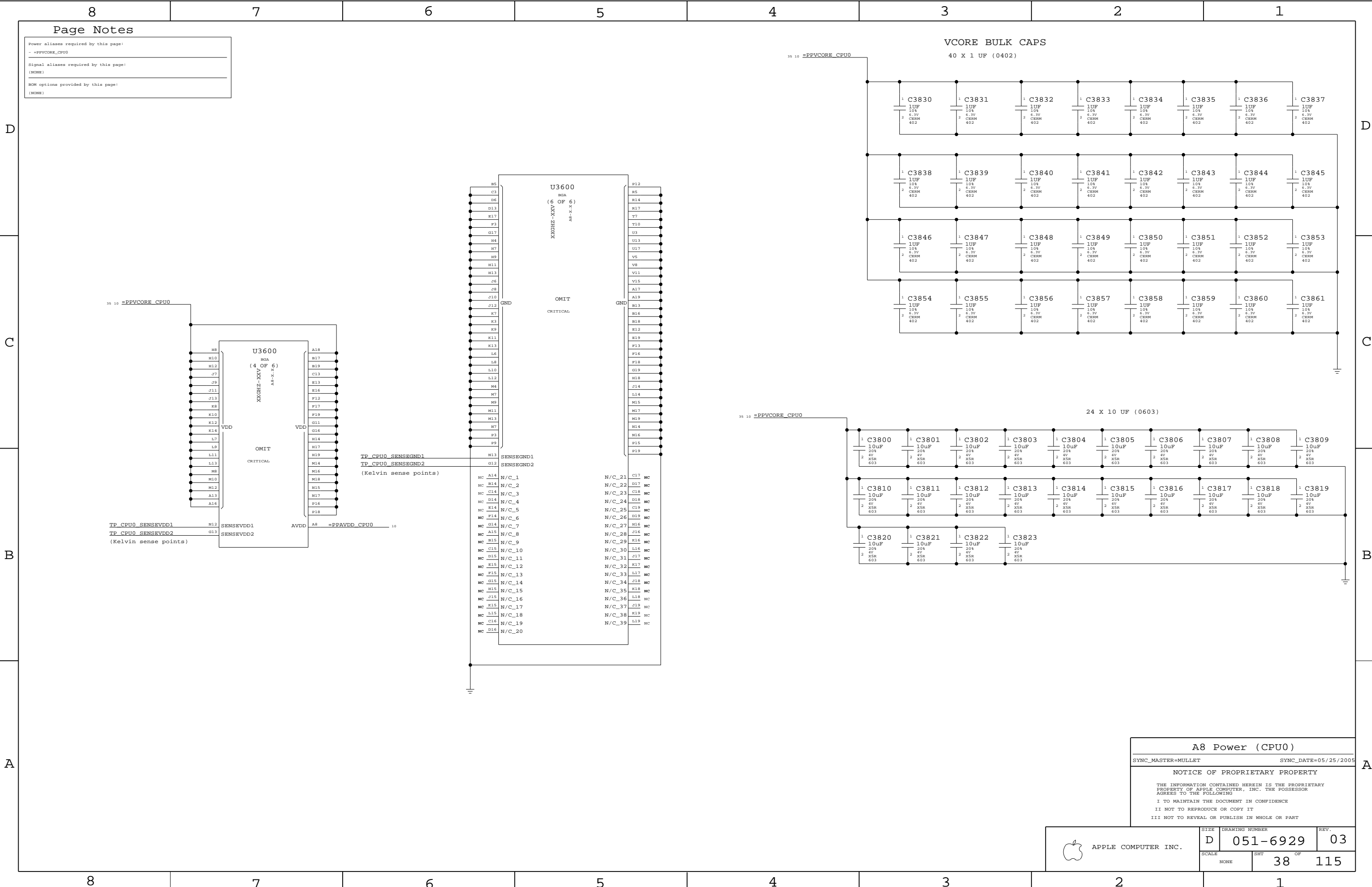
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	D	051-6929	03
SCALE		SHT	OF
NONE		34	115







Power aliases required by this page:
- =PPVCORE_CPU0

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

VCORE BULK CAPS
40 X 1 UF (0402)

24 X 10 UF (0603)

A8 Power (CPU0)

SYNC_MASTER=MULLET SYNC_DATE=05/25/2005

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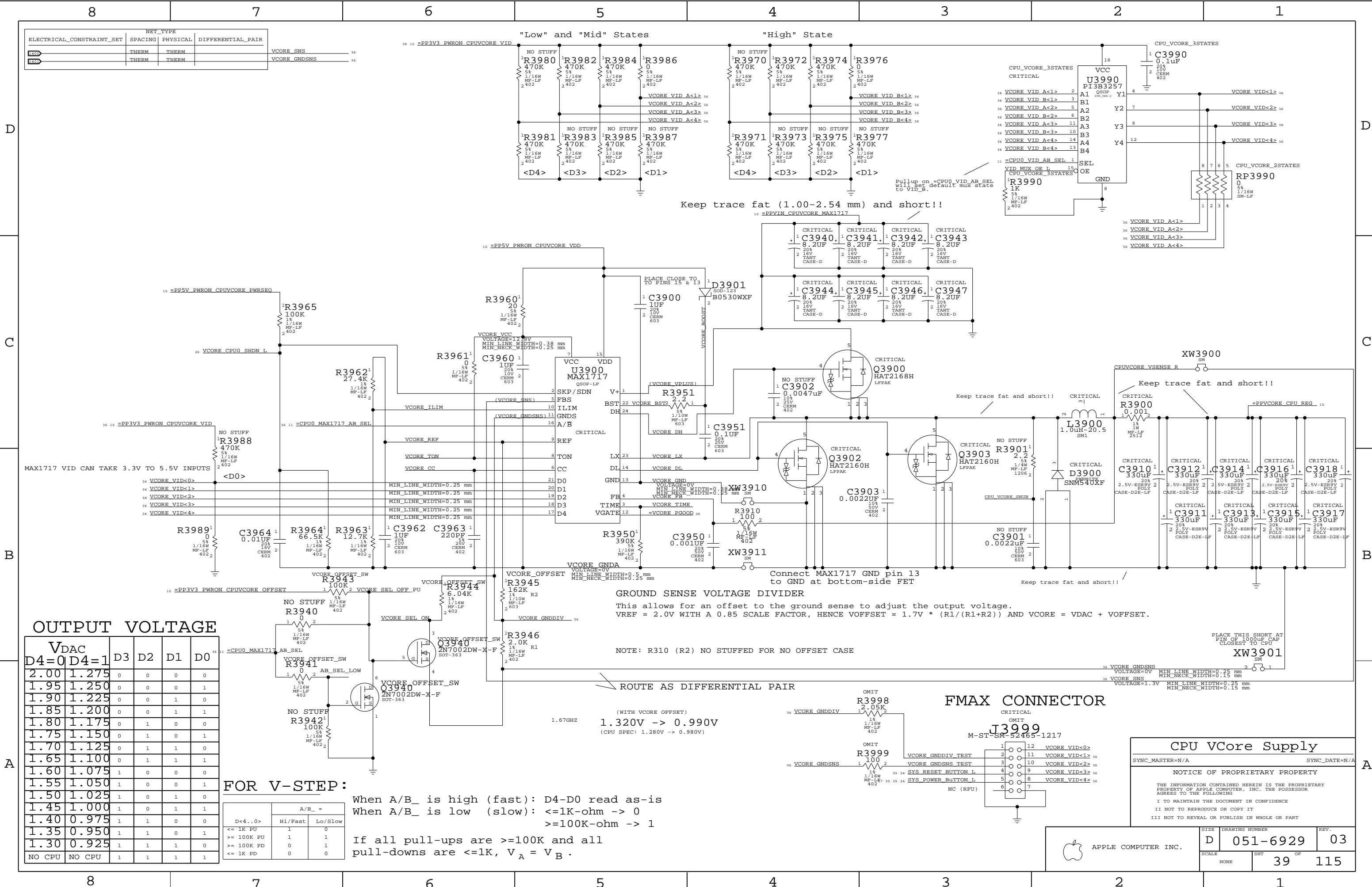
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	D	051-6929	03
SCALE	NONE	SHT	OF
		38	115



NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
R400	THERM	THERM	
R400	THERM	THERM	

D

D

C

C

B

B

A

A

OUTPUT VOLTAGE

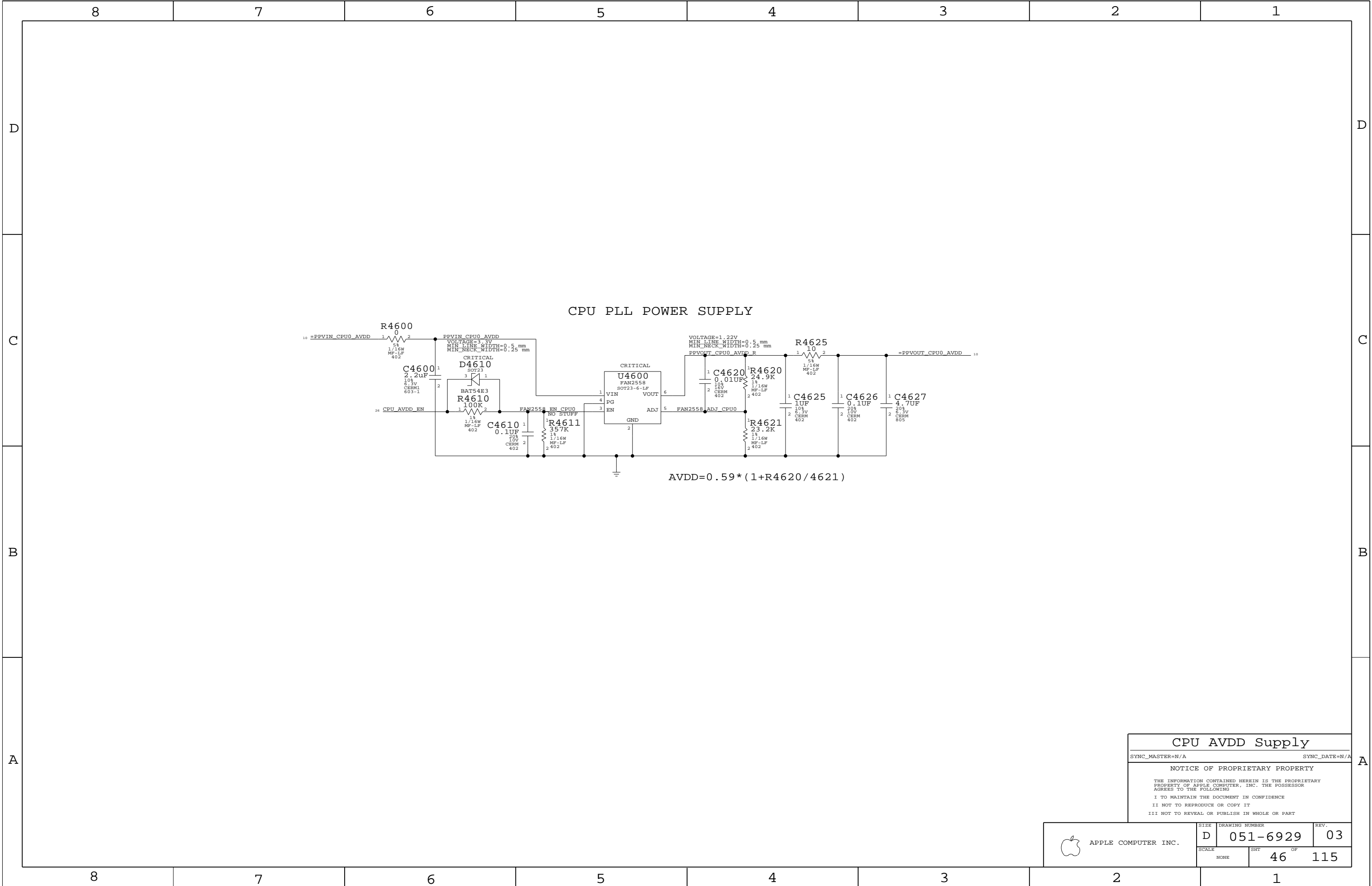
VDAC		D3	D2	D1	D0
D4=0	D4=1				
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

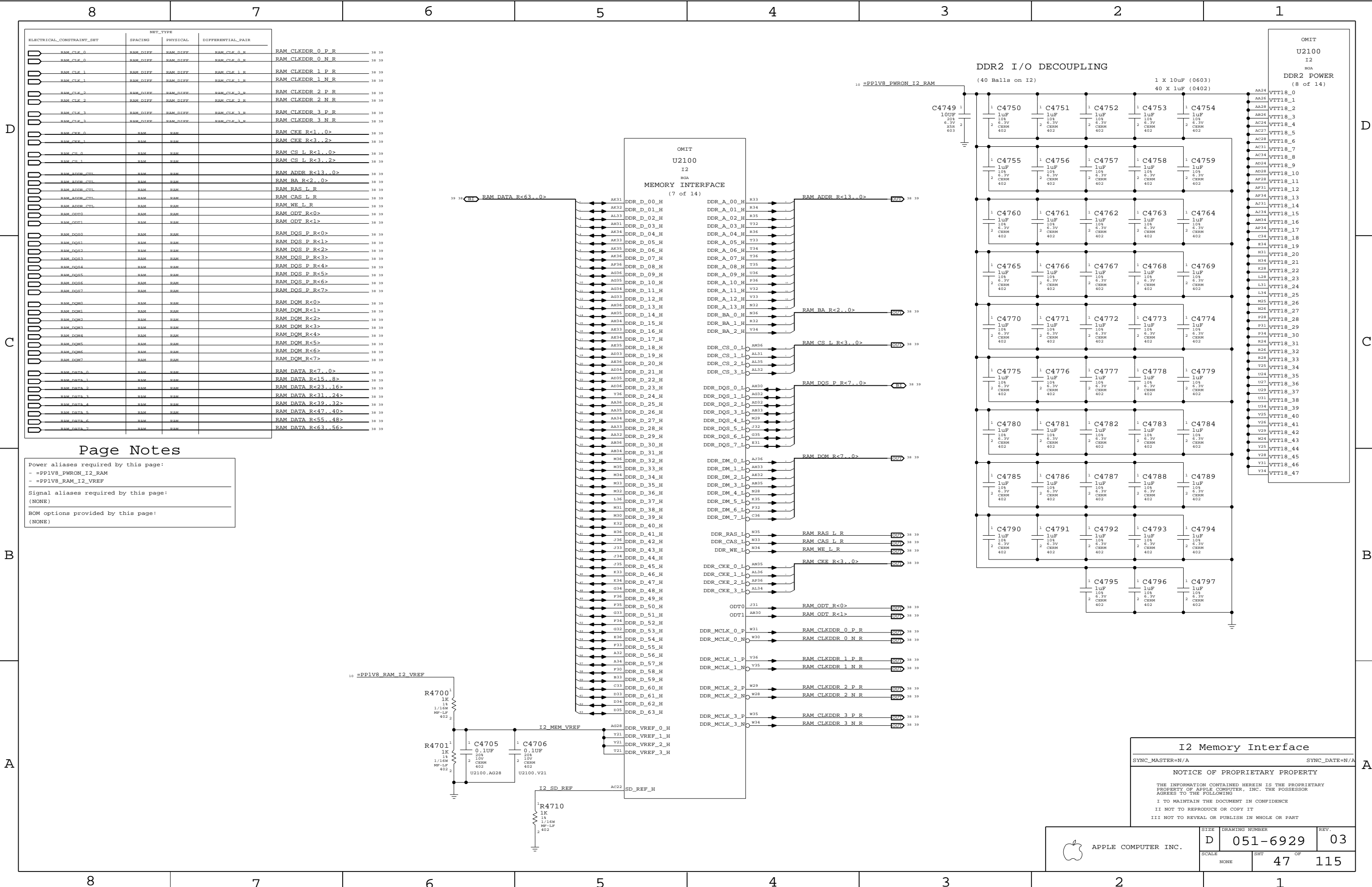
FOR V-STEP:

D<4..0>	A/B_ =	
	Hi/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, V_A = V_B.





NET_TYPE					
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
RAM_CLK_0	RAM_DIFF	RAM_DIFF	RAM_CLK_0_R	RAM_CLKDDR_0_P_R	38 39
RAM_CLK_0	RAM_DIFF	RAM_DIFF	RAM_CLK_0_R	RAM_CLKDDR_0_N_R	38 39
RAM_CLK_1	RAM_DIFF	RAM_DIFF	RAM_CLK_1_R	RAM_CLKDDR_1_P_R	38 39
RAM_CLK_1	RAM_DIFF	RAM_DIFF	RAM_CLK_1_R	RAM_CLKDDR_1_N_R	38 39
RAM_CLK_2	RAM_DIFF	RAM_DIFF	RAM_CLK_2_R	RAM_CLKDDR_2_P_R	38 39
RAM_CLK_2	RAM_DIFF	RAM_DIFF	RAM_CLK_2_R	RAM_CLKDDR_2_N_R	38 39
RAM_CLK_3	RAM_DIFF	RAM_DIFF	RAM_CLK_3_R	RAM_CLKDDR_3_P_R	38 39
RAM_CLK_3	RAM_DIFF	RAM_DIFF	RAM_CLK_3_R	RAM_CLKDDR_3_N_R	38 39
RAM_CKE_0	RAM	RAM		RAM_CKE_R<1..0>	38 39
RAM_CKE_1	RAM	RAM		RAM_CKE_R<3..2>	38 39
RAM_CS_0	RAM	RAM		RAM_CS_L_R<1..0>	38 39
RAM_CS_1	RAM	RAM		RAM_CS_L_R<3..2>	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_ADDR_R<13..0>	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_BA_R<2..0>	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_CAS_L_R	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_WE_L_R	38 39
RAM_ODT0	RAM	RAM		RAM_ODT_R<0>	38 39
RAM_ODT1	RAM	RAM		RAM_ODT_R<1>	38 39
RAM_DQS0	RAM	RAM		RAM_DQS_P_R<0>	38 39
RAM_DQS1	RAM	RAM		RAM_DQS_P_R<1>	38 39
RAM_DQS2	RAM	RAM		RAM_DQS_P_R<2>	38 39
RAM_DQS3	RAM	RAM		RAM_DQS_P_R<3>	38 39
RAM_DQS4	RAM	RAM		RAM_DQS_P_R<4>	38 39
RAM_DQS5	RAM	RAM		RAM_DQS_P_R<5>	38 39
RAM_DQS6	RAM	RAM		RAM_DQS_P_R<6>	38 39
RAM_DQS7	RAM	RAM		RAM_DQS_P_R<7>	38 39
RAM_DQM0	RAM	RAM		RAM_DQM_R<0>	38 39
RAM_DQM1	RAM	RAM		RAM_DQM_R<1>	38 39
RAM_DQM2	RAM	RAM		RAM_DQM_R<2>	38 39
RAM_DQM3	RAM	RAM		RAM_DQM_R<3>	38 39
RAM_DQM4	RAM	RAM		RAM_DQM_R<4>	38 39
RAM_DQM5	RAM	RAM		RAM_DQM_R<5>	38 39
RAM_DQM6	RAM	RAM		RAM_DQM_R<6>	38 39
RAM_DQM7	RAM	RAM		RAM_DQM_R<7>	38 39
RAM_DATA_0	RAM	RAM		RAM_DATA_R<7..0>	38 39
RAM_DATA_1	RAM	RAM		RAM_DATA_R<15..8>	38 39
RAM_DATA_2	RAM	RAM		RAM_DATA_R<23..16>	38 39
RAM_DATA_3	RAM	RAM		RAM_DATA_R<31..24>	38 39
RAM_DATA_4	RAM	RAM		RAM_DATA_R<39..32>	38 39
RAM_DATA_5	RAM	RAM		RAM_DATA_R<47..40>	38 39
RAM_DATA_6	RAM	RAM		RAM_DATA_R<55..48>	38 39
RAM_DATA_7	RAM	RAM		RAM_DATA_R<63..56>	38 39

Power aliases required by this page:
- =PP1V8_PWRON_I2_RAM
- =PP1V8_RAM_I2_VREF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

A

B

C

D

I2 Memory Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	NONE		47 OF 115

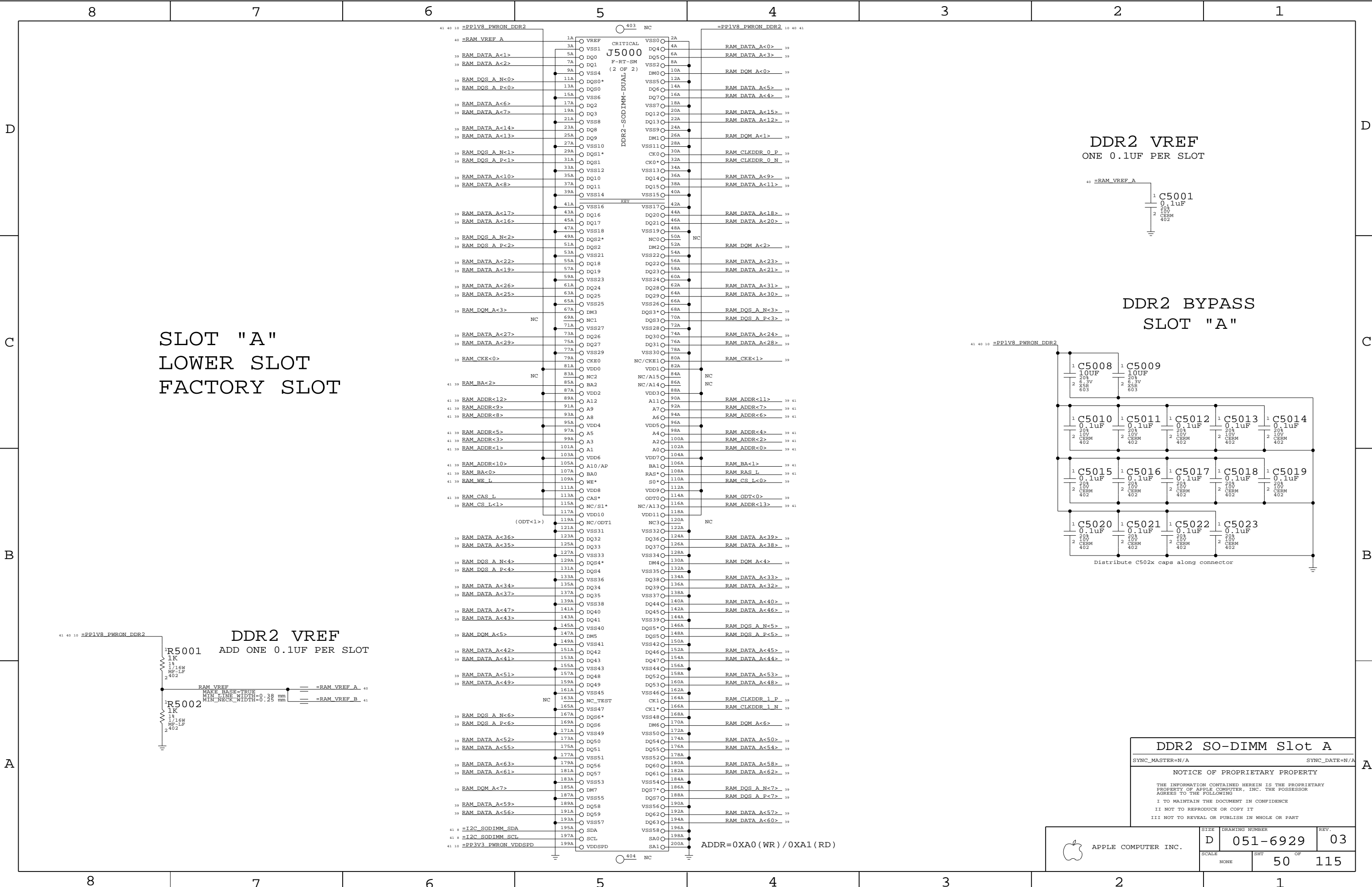
D

C

B

38DA

APPLE COMPUTER INC.



SLOT "A"
LOWER SLOT
FACTORY SLOT

DDR2 VREF
ONE 0.1UF PER SLOT

DDR2 BYPASS
SLOT "A"

DDR2 SO-DIMM Slot A

SYNC_MASTER=N/A SYNC_DATE=N/A

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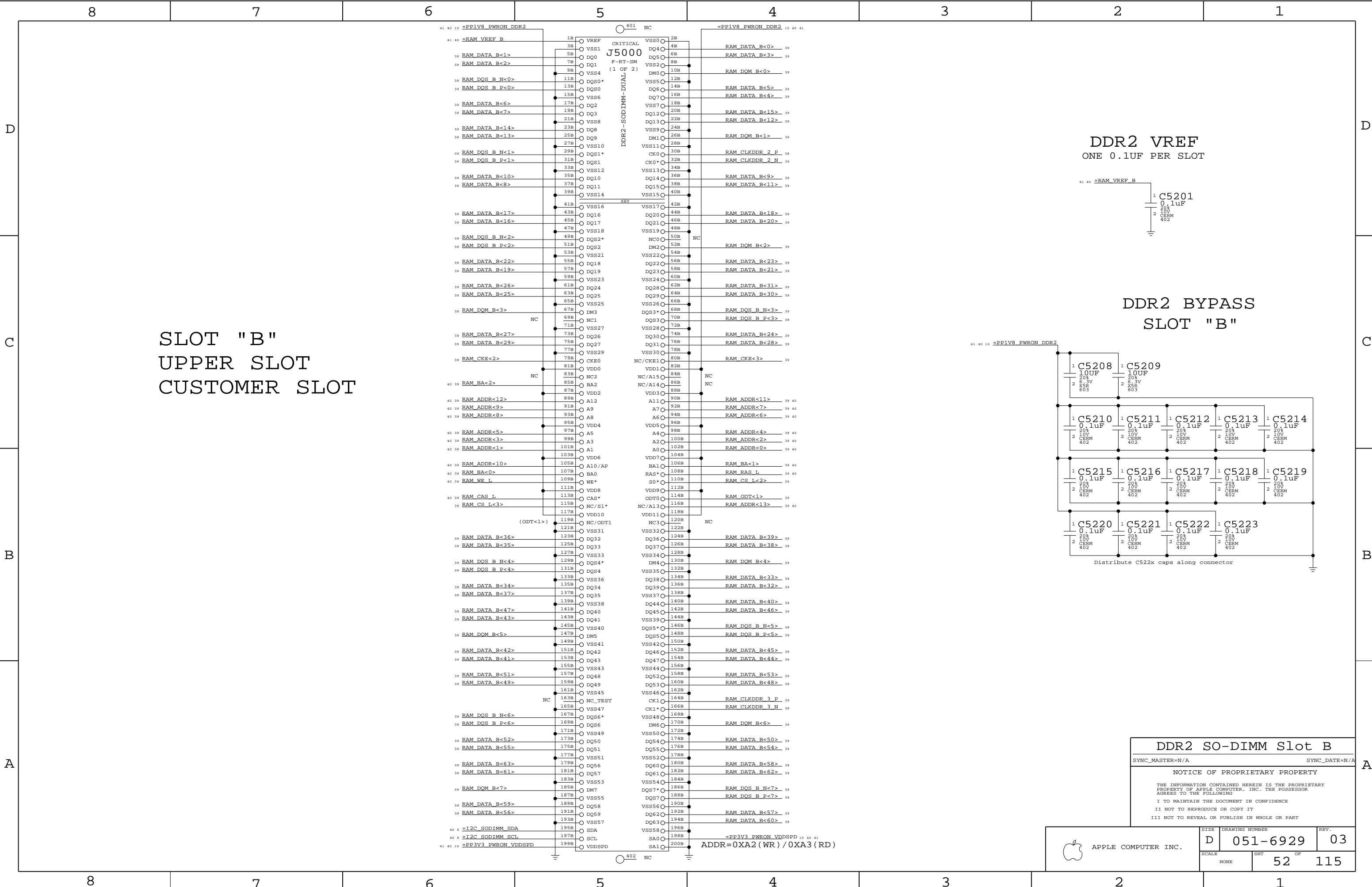
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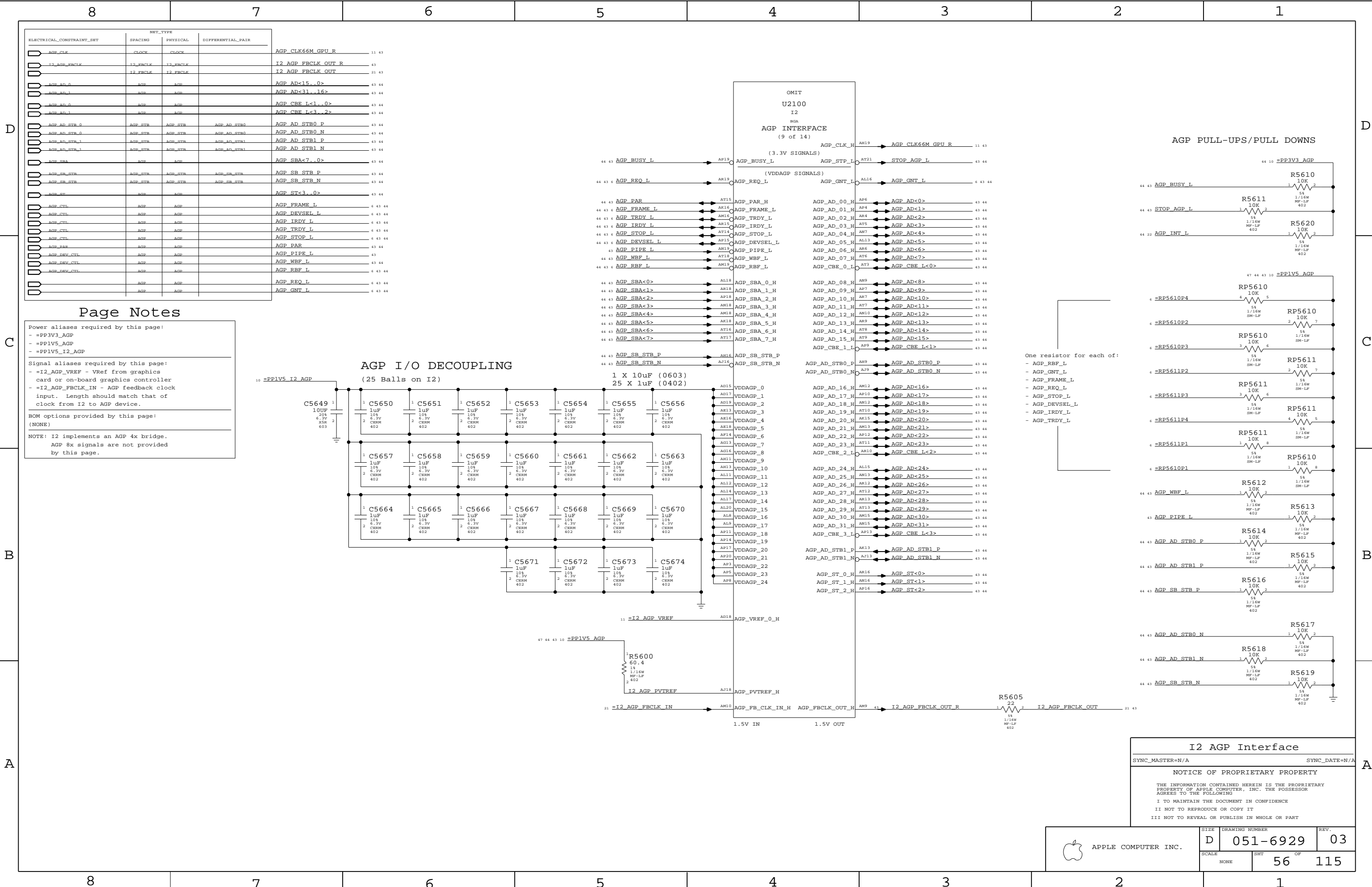


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	50	115



8		7		6		5		4		3		2		1																																																																																																																																																																																																																								
D	<table><tr><th colspan="4">NET_TYPE</th></tr><tr><th>ELECTRICAL_CONSTRAINT_SET</th><th>SPACING</th><th>PHYSICAL</th><th>DIFFERENTIAL_PAIR</th></tr></table>				NET_TYPE				ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	<table><tr><td>R105</td><td>FB_A_CLK_0</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_A_CLK_0_R</td><td>FB_A_CLKDDR_0_P_R</td></tr><tr><td>R106</td><td>(provided above)</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_A_CLK_0_R</td><td>FB_A_CLKDDR_0_N_R</td></tr><tr><td>R107</td><td>FB_A_CLK_1</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_A_CLK_1_R</td><td>FB_A_CLKDDR_1_P_R</td></tr><tr><td>R108</td><td>(provided above)</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_A_CLK_1_R</td><td>FB_A_CLKDDR_1_N_R</td></tr><tr><td>R109</td><td>FB_A_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_CKE_R</td></tr><tr><td>R110</td><td>FB_A_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_CS_L_R</td></tr><tr><td>R111</td><td>FB_A_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_ADDR_R<12..0></td></tr><tr><td>R112</td><td>FB_A_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_BA_R<2..0></td></tr><tr><td>R113</td><td>FB_A_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_RAS_L_R</td></tr><tr><td>R114</td><td>FB_A_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_CAS_L_R</td></tr><tr><td>R115</td><td>FB_A_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_WE_L_R</td></tr><tr><td>R116</td><td>FB_A_DQS0</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQS_R<0></td></tr><tr><td>R117</td><td>FB_A_DQS1</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQS_R<1></td></tr><tr><td>R118</td><td>FB_A_DQS2</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQS_R<2></td></tr><tr><td>R119</td><td>FB_A_DQS3</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQS_R<3></td></tr><tr><td>R120</td><td>FB_A_DQS4</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQS_R<4></td></tr><tr><td>R121</td><td>FB_A_DQS5</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQS_R<5></td></tr><tr><td>R122</td><td>FB_A_DQS6</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQS_R<6></td></tr><tr><td>R123</td><td>FB_A_DQS7</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQS_R<7></td></tr><tr><td>R124</td><td>FB_A_DQM0</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQM_R<0></td></tr><tr><td>R125</td><td>FB_A_DQM1</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQM_R<1></td></tr><tr><td>R126</td><td>FB_A_DQM2</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQM_R<2></td></tr><tr><td>R127</td><td>FB_A_DQM3</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQM_R<3></td></tr><tr><td>R128</td><td>FB_A_DQM4</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQM_R<4></td></tr><tr><td>R129</td><td>FB_A_DQM5</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQM_R<5></td></tr><tr><td>R130</td><td>FB_A_DQM6</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQM_R<6></td></tr><tr><td>R131</td><td>FB_A_DQM7</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQM_R<7></td></tr><tr><td>R132</td><td>FB_A_DQ0</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQ_R<7..0></td></tr><tr><td>R133</td><td>FB_A_DQ1</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQ_R<15..8></td></tr><tr><td>R134</td><td>FB_A_DQ2</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQ_R<23..16></td></tr><tr><td>R135</td><td>FB_A_DQ3</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQ_R<31..24></td></tr><tr><td>R136</td><td>FB_A_DQ4</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQ_R<39..32></td></tr><tr><td>R137</td><td>FB_A_DQ5</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQ_R<47..40></td></tr><tr><td>R138</td><td>FB_A_DQ6</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQ_R<55..48></td></tr><tr><td>R139</td><td>FB_A_DQ7</td><td>RAM</td><td>RAM</td><td></td><td>FB_A_DQ_R<63..56></td></tr></table>				R105	FB_A_CLK_0	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB_A_CLKDDR_0_P_R	R106	(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB_A_CLKDDR_0_N_R	R107	FB_A_CLK_1	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB_A_CLKDDR_1_P_R	R108	(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB_A_CLKDDR_1_N_R	R109	FB_A_ADDR_CTL	RAM	RAM		FB_A_CKE_R	R110	FB_A_ADDR_CTL	RAM	RAM		FB_A_CS_L_R	R111	FB_A_ADDR_CTL	RAM	RAM		FB_A_ADDR_R<12..0>	R112	FB_A_ADDR_CTL	RAM	RAM		FB_A_BA_R<2..0>	R113	FB_A_ADDR_CTL	RAM	RAM		FB_A_RAS_L_R	R114	FB_A_ADDR_CTL	RAM	RAM		FB_A_CAS_L_R	R115	FB_A_ADDR_CTL	RAM	RAM		FB_A_WE_L_R	R116	FB_A_DQS0	RAM	RAM		FB_A_DQS_R<0>	R117	FB_A_DQS1	RAM	RAM		FB_A_DQS_R<1>	R118	FB_A_DQS2	RAM	RAM		FB_A_DQS_R<2>	R119	FB_A_DQS3	RAM	RAM		FB_A_DQS_R<3>	R120	FB_A_DQS4	RAM	RAM		FB_A_DQS_R<4>	R121	FB_A_DQS5	RAM	RAM		FB_A_DQS_R<5>	R122	FB_A_DQS6	RAM	RAM		FB_A_DQS_R<6>	R123	FB_A_DQS7	RAM	RAM		FB_A_DQS_R<7>	R124	FB_A_DQM0	RAM	RAM		FB_A_DQM_R<0>	R125	FB_A_DQM1	RAM	RAM		FB_A_DQM_R<1>	R126	FB_A_DQM2	RAM	RAM		FB_A_DQM_R<2>	R127	FB_A_DQM3	RAM	RAM		FB_A_DQM_R<3>	R128	FB_A_DQM4	RAM	RAM		FB_A_DQM_R<4>	R129	FB_A_DQM5	RAM	RAM		FB_A_DQM_R<5>	R130	FB_A_DQM6	RAM	RAM		FB_A_DQM_R<6>	R131	FB_A_DQM7	RAM	RAM		FB_A_DQM_R<7>	R132	FB_A_DQ0	RAM	RAM		FB_A_DQ_R<7..0>	R133	FB_A_DQ1	RAM	RAM		FB_A_DQ_R<15..8>	R134	FB_A_DQ2	RAM	RAM		FB_A_DQ_R<23..16>	R135	FB_A_DQ3	RAM	RAM		FB_A_DQ_R<31..24>	R136	FB_A_DQ4	RAM	RAM		FB_A_DQ_R<39..32>	R137	FB_A_DQ5	RAM	RAM		FB_A_DQ_R<47..40>	R138	FB_A_DQ6	RAM	RAM		FB_A_DQ_R<55..48>	R139	FB_A_DQ7	RAM	RAM		FB_A_DQ_R<63..56>				
	NET_TYPE																																																																																																																																																																																																																																					
	ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR																																																																																																																																																																																																																																		
	R105	FB_A_CLK_0	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB_A_CLKDDR_0_P_R																																																																																																																																																																																																																																
	R106	(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB_A_CLKDDR_0_N_R																																																																																																																																																																																																																																
	R107	FB_A_CLK_1	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB_A_CLKDDR_1_P_R																																																																																																																																																																																																																																
	R108	(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB_A_CLKDDR_1_N_R																																																																																																																																																																																																																																
	R109	FB_A_ADDR_CTL	RAM	RAM		FB_A_CKE_R																																																																																																																																																																																																																																
	R110	FB_A_ADDR_CTL	RAM	RAM		FB_A_CS_L_R																																																																																																																																																																																																																																
	R111	FB_A_ADDR_CTL	RAM	RAM		FB_A_ADDR_R<12..0>																																																																																																																																																																																																																																
	R112	FB_A_ADDR_CTL	RAM	RAM		FB_A_BA_R<2..0>																																																																																																																																																																																																																																
	R113	FB_A_ADDR_CTL	RAM	RAM		FB_A_RAS_L_R																																																																																																																																																																																																																																
	R114	FB_A_ADDR_CTL	RAM	RAM		FB_A_CAS_L_R																																																																																																																																																																																																																																
	R115	FB_A_ADDR_CTL	RAM	RAM		FB_A_WE_L_R																																																																																																																																																																																																																																
	R116	FB_A_DQS0	RAM	RAM		FB_A_DQS_R<0>																																																																																																																																																																																																																																
	R117	FB_A_DQS1	RAM	RAM		FB_A_DQS_R<1>																																																																																																																																																																																																																																
	R118	FB_A_DQS2	RAM	RAM		FB_A_DQS_R<2>																																																																																																																																																																																																																																
	R119	FB_A_DQS3	RAM	RAM		FB_A_DQS_R<3>																																																																																																																																																																																																																																
	R120	FB_A_DQS4	RAM	RAM		FB_A_DQS_R<4>																																																																																																																																																																																																																																
	R121	FB_A_DQS5	RAM	RAM		FB_A_DQS_R<5>																																																																																																																																																																																																																																
	R122	FB_A_DQS6	RAM	RAM		FB_A_DQS_R<6>																																																																																																																																																																																																																																
	R123	FB_A_DQS7	RAM	RAM		FB_A_DQS_R<7>																																																																																																																																																																																																																																
	R124	FB_A_DQM0	RAM	RAM		FB_A_DQM_R<0>																																																																																																																																																																																																																																
	R125	FB_A_DQM1	RAM	RAM		FB_A_DQM_R<1>																																																																																																																																																																																																																																
	R126	FB_A_DQM2	RAM	RAM		FB_A_DQM_R<2>																																																																																																																																																																																																																																
	R127	FB_A_DQM3	RAM	RAM		FB_A_DQM_R<3>																																																																																																																																																																																																																																
	R128	FB_A_DQM4	RAM	RAM		FB_A_DQM_R<4>																																																																																																																																																																																																																																
	R129	FB_A_DQM5	RAM	RAM		FB_A_DQM_R<5>																																																																																																																																																																																																																																
	R130	FB_A_DQM6	RAM	RAM		FB_A_DQM_R<6>																																																																																																																																																																																																																																
	R131	FB_A_DQM7	RAM	RAM		FB_A_DQM_R<7>																																																																																																																																																																																																																																
	R132	FB_A_DQ0	RAM	RAM		FB_A_DQ_R<7..0>																																																																																																																																																																																																																																
	R133	FB_A_DQ1	RAM	RAM		FB_A_DQ_R<15..8>																																																																																																																																																																																																																																
	R134	FB_A_DQ2	RAM	RAM		FB_A_DQ_R<23..16>																																																																																																																																																																																																																																
	R135	FB_A_DQ3	RAM	RAM		FB_A_DQ_R<31..24>																																																																																																																																																																																																																																
	R136	FB_A_DQ4	RAM	RAM		FB_A_DQ_R<39..32>																																																																																																																																																																																																																																
	R137	FB_A_DQ5	RAM	RAM		FB_A_DQ_R<47..40>																																																																																																																																																																																																																																
	R138	FB_A_DQ6	RAM	RAM		FB_A_DQ_R<55..48>																																																																																																																																																																																																																																
	R139	FB_A_DQ7	RAM	RAM		FB_A_DQ_R<63..56>																																																																																																																																																																																																																																
	C	<table><tr><th colspan="4">NET_TYPE</th></tr><tr><th>ELECTRICAL_CONSTRAINT_SET</th><th>SPACING</th><th>PHYSICAL</th><th>DIFFERENTIAL_PAIR</th></tr></table>				NET_TYPE				ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	<table><tr><td>R140</td><td>FB_B_CLK_0</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_B_CLK_0_R</td><td>FB_B_CLKDDR_0_P_R</td></tr><tr><td>R141</td><td>(provided above)</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_B_CLK_0_R</td><td>FB_B_CLKDDR_0_N_R</td></tr><tr><td>R142</td><td>FB_B_CLK_1</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_B_CLK_1_R</td><td>FB_B_CLKDDR_1_P_R</td></tr><tr><td>R143</td><td>(provided above)</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_B_CLK_1_R</td><td>FB_B_CLKDDR_1_N_R</td></tr><tr><td>R144</td><td>FB_B_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_CKE_R</td></tr><tr><td>R145</td><td>FB_B_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_CS_L_R</td></tr><tr><td>R146</td><td>FB_B_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_ADDR_R<12..0></td></tr><tr><td>R147</td><td>FB_B_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_BA_R<2..0></td></tr><tr><td>R148</td><td>FB_B_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_RAS_L_R</td></tr><tr><td>R149</td><td>FB_B_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_CAS_L_R</td></tr><tr><td>R150</td><td>FB_B_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_WE_L_R</td></tr><tr><td>R151</td><td>FB_B_DQS0</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQS_R<0></td></tr><tr><td>R152</td><td>FB_B_DQS1</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQS_R<1></td></tr><tr><td>R153</td><td>FB_B_DQS2</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQS_R<2></td></tr><tr><td>R154</td><td>FB_B_DQS3</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQS_R<3></td></tr><tr><td>R155</td><td>FB_B_DQS4</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQS_R<4></td></tr><tr><td>R156</td><td>FB_B_DQS5</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQS_R<5></td></tr><tr><td>R157</td><td>FB_B_DQS6</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQS_R<6></td></tr><tr><td>R158</td><td>FB_B_DQS7</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQS_R<7></td></tr><tr><td>R159</td><td>FB_B_DQM0</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQM_R<0></td></tr><tr><td>R160</td><td>FB_B_DQM1</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQM_R<1></td></tr><tr><td>R161</td><td>FB_B_DQM2</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQM_R<2></td></tr><tr><td>R162</td><td>FB_B_DQM3</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQM_R<3></td></tr><tr><td>R163</td><td>FB_B_DQM4</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQM_R<4></td></tr><tr><td>R164</td><td>FB_B_DQM5</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQM_R<5></td></tr><tr><td>R165</td><td>FB_B_DQM6</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQM_R<6></td></tr><tr><td>R166</td><td>FB_B_DQM7</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQM_R<7></td></tr><tr><td>R167</td><td>FB_B_DQ0</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQ_R<7..0></td></tr><tr><td>R168</td><td>FB_B_DQ1</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQ_R<15..8></td></tr><tr><td>R169</td><td>FB_B_DQ2</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQ_R<23..16></td></tr><tr><td>R170</td><td>FB_B_DQ3</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQ_R<31..24></td></tr><tr><td>R171</td><td>FB_B_DQ4</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQ_R<39..32></td></tr><tr><td>R172</td><td>FB_B_DQ5</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQ_R<47..40></td></tr><tr><td>R173</td><td>FB_B_DQ6</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQ_R<55..48></td></tr><tr><td>R174</td><td>FB_B_DQ7</td><td>RAM</td><td>RAM</td><td></td><td>FB_B_DQ_R<63..56></td></tr></table>				R140	FB_B_CLK_0	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB_B_CLKDDR_0_P_R	R141	(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB_B_CLKDDR_0_N_R	R142	FB_B_CLK_1	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB_B_CLKDDR_1_P_R	R143	(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB_B_CLKDDR_1_N_R	R144	FB_B_ADDR_CTL	RAM	RAM		FB_B_CKE_R	R145	FB_B_ADDR_CTL	RAM	RAM		FB_B_CS_L_R	R146	FB_B_ADDR_CTL	RAM	RAM		FB_B_ADDR_R<12..0>	R147	FB_B_ADDR_CTL	RAM	RAM		FB_B_BA_R<2..0>	R148	FB_B_ADDR_CTL	RAM	RAM		FB_B_RAS_L_R	R149	FB_B_ADDR_CTL	RAM	RAM		FB_B_CAS_L_R	R150	FB_B_ADDR_CTL	RAM	RAM		FB_B_WE_L_R	R151	FB_B_DQS0	RAM	RAM		FB_B_DQS_R<0>	R152	FB_B_DQS1	RAM	RAM		FB_B_DQS_R<1>	R153	FB_B_DQS2	RAM	RAM		FB_B_DQS_R<2>	R154	FB_B_DQS3	RAM	RAM		FB_B_DQS_R<3>	R155	FB_B_DQS4	RAM	RAM		FB_B_DQS_R<4>	R156	FB_B_DQS5	RAM	RAM		FB_B_DQS_R<5>	R157	FB_B_DQS6	RAM	RAM		FB_B_DQS_R<6>	R158	FB_B_DQS7	RAM	RAM		FB_B_DQS_R<7>	R159	FB_B_DQM0	RAM	RAM		FB_B_DQM_R<0>	R160	FB_B_DQM1	RAM	RAM		FB_B_DQM_R<1>	R161	FB_B_DQM2	RAM	RAM		FB_B_DQM_R<2>	R162	FB_B_DQM3	RAM	RAM		FB_B_DQM_R<3>	R163	FB_B_DQM4	RAM	RAM		FB_B_DQM_R<4>	R164	FB_B_DQM5	RAM	RAM		FB_B_DQM_R<5>	R165	FB_B_DQM6	RAM	RAM		FB_B_DQM_R<6>	R166	FB_B_DQM7	RAM	RAM		FB_B_DQM_R<7>	R167	FB_B_DQ0	RAM	RAM		FB_B_DQ_R<7..0>	R168	FB_B_DQ1	RAM	RAM		FB_B_DQ_R<15..8>	R169	FB_B_DQ2	RAM	RAM		FB_B_DQ_R<23..16>	R170	FB_B_DQ3	RAM	RAM		FB_B_DQ_R<31..24>	R171	FB_B_DQ4	RAM	RAM		FB_B_DQ_R<39..32>	R172	FB_B_DQ5	RAM	RAM		FB_B_DQ_R<47..40>	R173	FB_B_DQ6	RAM	RAM		FB_B_DQ_R<55..48>	R174	FB_B_DQ7	RAM	RAM		FB_B_DQ_R<63..56>			
NET_TYPE																																																																																																																																																																																																																																						
ELECTRICAL_CONSTRAINT_SET		SPACING	PHYSICAL	DIFFERENTIAL_PAIR																																																																																																																																																																																																																																		
R140		FB_B_CLK_0	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB_B_CLKDDR_0_P_R																																																																																																																																																																																																																																
R141		(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB_B_CLKDDR_0_N_R																																																																																																																																																																																																																																
R142		FB_B_CLK_1	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB_B_CLKDDR_1_P_R																																																																																																																																																																																																																																
R143		(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB_B_CLKDDR_1_N_R																																																																																																																																																																																																																																
R144		FB_B_ADDR_CTL	RAM	RAM		FB_B_CKE_R																																																																																																																																																																																																																																
R145		FB_B_ADDR_CTL	RAM	RAM		FB_B_CS_L_R																																																																																																																																																																																																																																
R146		FB_B_ADDR_CTL	RAM	RAM		FB_B_ADDR_R<12..0>																																																																																																																																																																																																																																
R147		FB_B_ADDR_CTL	RAM	RAM		FB_B_BA_R<2..0>																																																																																																																																																																																																																																
R148		FB_B_ADDR_CTL	RAM	RAM		FB_B_RAS_L_R																																																																																																																																																																																																																																
R149		FB_B_ADDR_CTL	RAM	RAM		FB_B_CAS_L_R																																																																																																																																																																																																																																
R150		FB_B_ADDR_CTL	RAM	RAM		FB_B_WE_L_R																																																																																																																																																																																																																																
R151		FB_B_DQS0	RAM	RAM		FB_B_DQS_R<0>																																																																																																																																																																																																																																
R152		FB_B_DQS1	RAM	RAM		FB_B_DQS_R<1>																																																																																																																																																																																																																																
R153		FB_B_DQS2	RAM	RAM		FB_B_DQS_R<2>																																																																																																																																																																																																																																
R154		FB_B_DQS3	RAM	RAM		FB_B_DQS_R<3>																																																																																																																																																																																																																																
R155		FB_B_DQS4	RAM	RAM		FB_B_DQS_R<4>																																																																																																																																																																																																																																
R156		FB_B_DQS5	RAM	RAM		FB_B_DQS_R<5>																																																																																																																																																																																																																																
R157		FB_B_DQS6	RAM	RAM		FB_B_DQS_R<6>																																																																																																																																																																																																																																
R158		FB_B_DQS7	RAM	RAM		FB_B_DQS_R<7>																																																																																																																																																																																																																																
R159		FB_B_DQM0	RAM	RAM		FB_B_DQM_R<0>																																																																																																																																																																																																																																
R160		FB_B_DQM1	RAM	RAM		FB_B_DQM_R<1>																																																																																																																																																																																																																																
R161		FB_B_DQM2	RAM	RAM		FB_B_DQM_R<2>																																																																																																																																																																																																																																
R162		FB_B_DQM3	RAM	RAM		FB_B_DQM_R<3>																																																																																																																																																																																																																																
R163		FB_B_DQM4	RAM	RAM		FB_B_DQM_R<4>																																																																																																																																																																																																																																
R164		FB_B_DQM5	RAM	RAM		FB_B_DQM_R<5>																																																																																																																																																																																																																																
R165		FB_B_DQM6	RAM	RAM		FB_B_DQM_R<6>																																																																																																																																																																																																																																
R166		FB_B_DQM7	RAM	RAM		FB_B_DQM_R<7>																																																																																																																																																																																																																																
R167		FB_B_DQ0	RAM	RAM		FB_B_DQ_R<7..0>																																																																																																																																																																																																																																
R168		FB_B_DQ1	RAM	RAM		FB_B_DQ_R<15..8>																																																																																																																																																																																																																																
R169		FB_B_DQ2	RAM	RAM		FB_B_DQ_R<23..16>																																																																																																																																																																																																																																
R170		FB_B_DQ3	RAM	RAM		FB_B_DQ_R<31..24>																																																																																																																																																																																																																																
R171		FB_B_DQ4	RAM	RAM		FB_B_DQ_R<39..32>																																																																																																																																																																																																																																
R172		FB_B_DQ5	RAM	RAM		FB_B_DQ_R<47..40>																																																																																																																																																																																																																																
R173		FB_B_DQ6	RAM	RAM		FB_B_DQ_R<55..48>																																																																																																																																																																																																																																
R174		FB_B_DQ7	RAM	RAM		FB_B_DQ_R<63..56>																																																																																																																																																																																																																																
B		<table><tr><th colspan="4">NET_TYPE</th></tr><tr><th>ELECTRICAL_CONSTRAINT_SET</th><th>SPACING</th><th>PHYSICAL</th><th>DIFFERENTIAL_PAIR</th></tr></table>				NET_TYPE				ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	<table><tr><td>R175</td><td>FB_C_CLK_0</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_C_CLK_0_R</td><td>FB_C_CLKDDR_0_P_R</td></tr><tr><td>R176</td><td>(provided above)</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_C_CLK_0_R</td><td>FB_C_CLKDDR_0_N_R</td></tr><tr><td>R177</td><td>FB_C_CLK_1</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_C_CLK_1_R</td><td>FB_C_CLKDDR_1_P_R</td></tr><tr><td>R178</td><td>(provided above)</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_C_CLK_1_R</td><td>FB_C_CLKDDR_1_N_R</td></tr><tr><td>R179</td><td>FB_C_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_CKE_R</td></tr><tr><td>R180</td><td>FB_C_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_CS_L_R</td></tr><tr><td>R181</td><td>FB_C_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_ADDR_R<12..0></td></tr><tr><td>R182</td><td>FB_C_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_BA_R<2..0></td></tr><tr><td>R183</td><td>FB_C_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_RAS_L_R</td></tr><tr><td>R184</td><td>FB_C_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_CAS_L_R</td></tr><tr><td>R185</td><td>FB_C_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_WE_L_R</td></tr><tr><td>R186</td><td>FB_C_DQS0</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQS_R<0></td></tr><tr><td>R187</td><td>FB_C_DQS1</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQS_R<1></td></tr><tr><td>R188</td><td>FB_C_DQS2</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQS_R<2></td></tr><tr><td>R189</td><td>FB_C_DQS3</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQS_R<3></td></tr><tr><td>R190</td><td>FB_C_DQS4</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQS_R<4></td></tr><tr><td>R191</td><td>FB_C_DQS5</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQS_R<5></td></tr><tr><td>R192</td><td>FB_C_DQS6</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQS_R<6></td></tr><tr><td>R193</td><td>FB_C_DQS7</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQS_R<7></td></tr><tr><td>R194</td><td>FB_C_DQM0</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQM_R<0></td></tr><tr><td>R195</td><td>FB_C_DQM1</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQM_R<1></td></tr><tr><td>R196</td><td>FB_C_DQM2</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQM_R<2></td></tr><tr><td>R197</td><td>FB_C_DQM3</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQM_R<3></td></tr><tr><td>R198</td><td>FB_C_DQM4</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQM_R<4></td></tr><tr><td>R199</td><td>FB_C_DQM5</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQM_R<5></td></tr><tr><td>R200</td><td>FB_C_DQM6</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQM_R<6></td></tr><tr><td>R201</td><td>FB_C_DQM7</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQM_R<7></td></tr><tr><td>R202</td><td>FB_C_DQ0</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQ_R<7..0></td></tr><tr><td>R203</td><td>FB_C_DQ1</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQ_R<15..8></td></tr><tr><td>R204</td><td>FB_C_DQ2</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQ_R<23..16></td></tr><tr><td>R205</td><td>FB_C_DQ3</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQ_R<31..24></td></tr><tr><td>R206</td><td>FB_C_DQ4</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQ_R<39..32></td></tr><tr><td>R207</td><td>FB_C_DQ5</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQ_R<47..40></td></tr><tr><td>R208</td><td>FB_C_DQ6</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQ_R<55..48></td></tr><tr><td>R209</td><td>FB_C_DQ7</td><td>RAM</td><td>RAM</td><td></td><td>FB_C_DQ_R<63..56></td></tr></table>				R175	FB_C_CLK_0	RAM_DIFF	RAM_DIFF	FB_C_CLK_0_R	FB_C_CLKDDR_0_P_R	R176	(provided above)	RAM_DIFF	RAM_DIFF	FB_C_CLK_0_R	FB_C_CLKDDR_0_N_R	R177	FB_C_CLK_1	RAM_DIFF	RAM_DIFF	FB_C_CLK_1_R	FB_C_CLKDDR_1_P_R	R178	(provided above)	RAM_DIFF	RAM_DIFF	FB_C_CLK_1_R	FB_C_CLKDDR_1_N_R	R179	FB_C_ADDR_CTL	RAM	RAM		FB_C_CKE_R	R180	FB_C_ADDR_CTL	RAM	RAM		FB_C_CS_L_R	R181	FB_C_ADDR_CTL	RAM	RAM		FB_C_ADDR_R<12..0>	R182	FB_C_ADDR_CTL	RAM	RAM		FB_C_BA_R<2..0>	R183	FB_C_ADDR_CTL	RAM	RAM		FB_C_RAS_L_R	R184	FB_C_ADDR_CTL	RAM	RAM		FB_C_CAS_L_R	R185	FB_C_ADDR_CTL	RAM	RAM		FB_C_WE_L_R	R186	FB_C_DQS0	RAM	RAM		FB_C_DQS_R<0>	R187	FB_C_DQS1	RAM	RAM		FB_C_DQS_R<1>	R188	FB_C_DQS2	RAM	RAM		FB_C_DQS_R<2>	R189	FB_C_DQS3	RAM	RAM		FB_C_DQS_R<3>	R190	FB_C_DQS4	RAM	RAM		FB_C_DQS_R<4>	R191	FB_C_DQS5	RAM	RAM		FB_C_DQS_R<5>	R192	FB_C_DQS6	RAM	RAM		FB_C_DQS_R<6>	R193	FB_C_DQS7	RAM	RAM		FB_C_DQS_R<7>	R194	FB_C_DQM0	RAM	RAM		FB_C_DQM_R<0>	R195	FB_C_DQM1	RAM	RAM		FB_C_DQM_R<1>	R196	FB_C_DQM2	RAM	RAM		FB_C_DQM_R<2>	R197	FB_C_DQM3	RAM	RAM		FB_C_DQM_R<3>	R198	FB_C_DQM4	RAM	RAM		FB_C_DQM_R<4>	R199	FB_C_DQM5	RAM	RAM		FB_C_DQM_R<5>	R200	FB_C_DQM6	RAM	RAM		FB_C_DQM_R<6>	R201	FB_C_DQM7	RAM	RAM		FB_C_DQM_R<7>	R202	FB_C_DQ0	RAM	RAM		FB_C_DQ_R<7..0>	R203	FB_C_DQ1	RAM	RAM		FB_C_DQ_R<15..8>	R204	FB_C_DQ2	RAM	RAM		FB_C_DQ_R<23..16>	R205	FB_C_DQ3	RAM	RAM		FB_C_DQ_R<31..24>	R206	FB_C_DQ4	RAM	RAM		FB_C_DQ_R<39..32>	R207	FB_C_DQ5	RAM	RAM		FB_C_DQ_R<47..40>	R208	FB_C_DQ6	RAM	RAM		FB_C_DQ_R<55..48>	R209	FB_C_DQ7	RAM	RAM		FB_C_DQ_R<63..56>			
	NET_TYPE																																																																																																																																																																																																																																					
	ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR																																																																																																																																																																																																																																		
	R175	FB_C_CLK_0	RAM_DIFF	RAM_DIFF	FB_C_CLK_0_R	FB_C_CLKDDR_0_P_R																																																																																																																																																																																																																																
	R176	(provided above)	RAM_DIFF	RAM_DIFF	FB_C_CLK_0_R	FB_C_CLKDDR_0_N_R																																																																																																																																																																																																																																
	R177	FB_C_CLK_1	RAM_DIFF	RAM_DIFF	FB_C_CLK_1_R	FB_C_CLKDDR_1_P_R																																																																																																																																																																																																																																
	R178	(provided above)	RAM_DIFF	RAM_DIFF	FB_C_CLK_1_R	FB_C_CLKDDR_1_N_R																																																																																																																																																																																																																																
	R179	FB_C_ADDR_CTL	RAM	RAM		FB_C_CKE_R																																																																																																																																																																																																																																
	R180	FB_C_ADDR_CTL	RAM	RAM		FB_C_CS_L_R																																																																																																																																																																																																																																
	R181	FB_C_ADDR_CTL	RAM	RAM		FB_C_ADDR_R<12..0>																																																																																																																																																																																																																																
	R182	FB_C_ADDR_CTL	RAM	RAM		FB_C_BA_R<2..0>																																																																																																																																																																																																																																
	R183	FB_C_ADDR_CTL	RAM	RAM		FB_C_RAS_L_R																																																																																																																																																																																																																																
	R184	FB_C_ADDR_CTL	RAM	RAM		FB_C_CAS_L_R																																																																																																																																																																																																																																
	R185	FB_C_ADDR_CTL	RAM	RAM		FB_C_WE_L_R																																																																																																																																																																																																																																
	R186	FB_C_DQS0	RAM	RAM		FB_C_DQS_R<0>																																																																																																																																																																																																																																
	R187	FB_C_DQS1	RAM	RAM		FB_C_DQS_R<1>																																																																																																																																																																																																																																
	R188	FB_C_DQS2	RAM	RAM		FB_C_DQS_R<2>																																																																																																																																																																																																																																
	R189	FB_C_DQS3	RAM	RAM		FB_C_DQS_R<3>																																																																																																																																																																																																																																
	R190	FB_C_DQS4	RAM	RAM		FB_C_DQS_R<4>																																																																																																																																																																																																																																
	R191	FB_C_DQS5	RAM	RAM		FB_C_DQS_R<5>																																																																																																																																																																																																																																
	R192	FB_C_DQS6	RAM	RAM		FB_C_DQS_R<6>																																																																																																																																																																																																																																
	R193	FB_C_DQS7	RAM	RAM		FB_C_DQS_R<7>																																																																																																																																																																																																																																
	R194	FB_C_DQM0	RAM	RAM		FB_C_DQM_R<0>																																																																																																																																																																																																																																
	R195	FB_C_DQM1	RAM	RAM		FB_C_DQM_R<1>																																																																																																																																																																																																																																
	R196	FB_C_DQM2	RAM	RAM		FB_C_DQM_R<2>																																																																																																																																																																																																																																
	R197	FB_C_DQM3	RAM	RAM		FB_C_DQM_R<3>																																																																																																																																																																																																																																
	R198	FB_C_DQM4	RAM	RAM		FB_C_DQM_R<4>																																																																																																																																																																																																																																
	R199	FB_C_DQM5	RAM	RAM		FB_C_DQM_R<5>																																																																																																																																																																																																																																
	R200	FB_C_DQM6	RAM	RAM		FB_C_DQM_R<6>																																																																																																																																																																																																																																
	R201	FB_C_DQM7	RAM	RAM		FB_C_DQM_R<7>																																																																																																																																																																																																																																
	R202	FB_C_DQ0	RAM	RAM		FB_C_DQ_R<7..0>																																																																																																																																																																																																																																
	R203	FB_C_DQ1	RAM	RAM		FB_C_DQ_R<15..8>																																																																																																																																																																																																																																
	R204	FB_C_DQ2	RAM	RAM		FB_C_DQ_R<23..16>																																																																																																																																																																																																																																
	R205	FB_C_DQ3	RAM	RAM		FB_C_DQ_R<31..24>																																																																																																																																																																																																																																
	R206	FB_C_DQ4	RAM	RAM		FB_C_DQ_R<39..32>																																																																																																																																																																																																																																
	R207	FB_C_DQ5	RAM	RAM		FB_C_DQ_R<47..40>																																																																																																																																																																																																																																
	R208	FB_C_DQ6	RAM	RAM		FB_C_DQ_R<55..48>																																																																																																																																																																																																																																
	R209	FB_C_DQ7	RAM	RAM		FB_C_DQ_R<63..56>																																																																																																																																																																																																																																
	A	<table><tr><th colspan="4">NET_TYPE</th></tr><tr><th>ELECTRICAL_CONSTRAINT_SET</th><th>SPACING</th><th>PHYSICAL</th><th>DIFFERENTIAL_PAIR</th></tr></table>				NET_TYPE				ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	<table><tr><td>R210</td><td>FB_D_CLK_0</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_D_CLK_0_R</td><td>FB_D_CLKDDR_0_P_R</td></tr><tr><td>R211</td><td>(provided above)</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_D_CLK_0_R</td><td>FB_D_CLKDDR_0_N_R</td></tr><tr><td>R212</td><td>FB_D_CLK_1</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_D_CLK_1_R</td><td>FB_D_CLKDDR_1_P_R</td></tr><tr><td>R213</td><td>(provided above)</td><td>RAM_DIFF</td><td>RAM_DIFF</td><td>FB_D_CLK_1_R</td><td>FB_D_CLKDDR_1_N_R</td></tr><tr><td>R214</td><td>FB_D_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_CKE_R</td></tr><tr><td>R215</td><td>FB_D_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_CS_L_R</td></tr><tr><td>R216</td><td>FB_D_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_ADDR_R<12..0></td></tr><tr><td>R217</td><td>FB_D_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_BA_R<2..0></td></tr><tr><td>R218</td><td>FB_D_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_RAS_L_R</td></tr><tr><td>R219</td><td>FB_D_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_CAS_L_R</td></tr><tr><td>R220</td><td>FB_D_ADDR_CTL</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_WE_L_R</td></tr><tr><td>R221</td><td>FB_D_DQS0</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQS_R<0></td></tr><tr><td>R222</td><td>FB_D_DQS1</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQS_R<1></td></tr><tr><td>R223</td><td>FB_D_DQS2</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQS_R<2></td></tr><tr><td>R224</td><td>FB_D_DQS3</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQS_R<3></td></tr><tr><td>R225</td><td>FB_D_DQS4</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQS_R<4></td></tr><tr><td>R226</td><td>FB_D_DQS5</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQS_R<5></td></tr><tr><td>R227</td><td>FB_D_DQS6</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQS_R<6></td></tr><tr><td>R228</td><td>FB_D_DQS7</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQS_R<7></td></tr><tr><td>R229</td><td>FB_D_DQM0</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQM_R<0></td></tr><tr><td>R230</td><td>FB_D_DQM1</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQM_R<1></td></tr><tr><td>R231</td><td>FB_D_DQM2</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQM_R<2></td></tr><tr><td>R232</td><td>FB_D_DQM3</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQM_R<3></td></tr><tr><td>R233</td><td>FB_D_DQM4</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQM_R<4></td></tr><tr><td>R234</td><td>FB_D_DQM5</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQM_R<5></td></tr><tr><td>R235</td><td>FB_D_DQM6</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQM_R<6></td></tr><tr><td>R236</td><td>FB_D_DQM7</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQM_R<7></td></tr><tr><td>R237</td><td>FB_D_DQ0</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQ_R<7..0></td></tr><tr><td>R238</td><td>FB_D_DQ1</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQ_R<15..8></td></tr><tr><td>R239</td><td>FB_D_DQ2</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQ_R<23..16></td></tr><tr><td>R240</td><td>FB_D_DQ3</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQ_R<31..24></td></tr><tr><td>R241</td><td>FB_D_DQ4</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQ_R<39..32></td></tr><tr><td>R242</td><td>FB_D_DQ5</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQ_R<47..40></td></tr><tr><td>R243</td><td>FB_D_DQ6</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQ_R<55..48></td></tr><tr><td>R244</td><td>FB_D_DQ7</td><td>RAM</td><td>RAM</td><td></td><td>FB_D_DQ_R<63..56></td></tr></table>				R210	FB_D_CLK_0	RAM_DIFF	RAM_DIFF	FB_D_CLK_0_R	FB_D_CLKDDR_0_P_R	R211	(provided above)	RAM_DIFF	RAM_DIFF	FB_D_CLK_0_R	FB_D_CLKDDR_0_N_R	R212	FB_D_CLK_1	RAM_DIFF	RAM_DIFF	FB_D_CLK_1_R	FB_D_CLKDDR_1_P_R	R213	(provided above)	RAM_DIFF	RAM_DIFF	FB_D_CLK_1_R	FB_D_CLKDDR_1_N_R	R214	FB_D_ADDR_CTL	RAM	RAM		FB_D_CKE_R	R215	FB_D_ADDR_CTL	RAM	RAM		FB_D_CS_L_R	R216	FB_D_ADDR_CTL	RAM	RAM		FB_D_ADDR_R<12..0>	R217	FB_D_ADDR_CTL	RAM	RAM		FB_D_BA_R<2..0>	R218	FB_D_ADDR_CTL	RAM	RAM		FB_D_RAS_L_R	R219	FB_D_ADDR_CTL	RAM	RAM		FB_D_CAS_L_R	R220	FB_D_ADDR_CTL	RAM	RAM		FB_D_WE_L_R	R221	FB_D_DQS0	RAM	RAM		FB_D_DQS_R<0>	R222	FB_D_DQS1	RAM	RAM		FB_D_DQS_R<1>	R223	FB_D_DQS2	RAM	RAM		FB_D_DQS_R<2>	R224	FB_D_DQS3	RAM	RAM		FB_D_DQS_R<3>	R225	FB_D_DQS4	RAM	RAM		FB_D_DQS_R<4>	R226	FB_D_DQS5	RAM	RAM		FB_D_DQS_R<5>	R227	FB_D_DQS6	RAM	RAM		FB_D_DQS_R<6>	R228	FB_D_DQS7	RAM	RAM		FB_D_DQS_R<7>	R229	FB_D_DQM0	RAM	RAM		FB_D_DQM_R<0>	R230	FB_D_DQM1	RAM	RAM		FB_D_DQM_R<1>	R231	FB_D_DQM2	RAM	RAM		FB_D_DQM_R<2>	R232	FB_D_DQM3	RAM	RAM		FB_D_DQM_R<3>	R233	FB_D_DQM4	RAM	RAM		FB_D_DQM_R<4>	R234	FB_D_DQM5	RAM	RAM		FB_D_DQM_R<5>	R235	FB_D_DQM6	RAM	RAM		FB_D_DQM_R<6>	R236	FB_D_DQM7	RAM	RAM		FB_D_DQM_R<7>	R237	FB_D_DQ0	RAM	RAM		FB_D_DQ_R<7..0>	R238	FB_D_DQ1	RAM	RAM		FB_D_DQ_R<15..8>	R239	FB_D_DQ2	RAM	RAM		FB_D_DQ_R<23..16>	R240	FB_D_DQ3	RAM	RAM		FB_D_DQ_R<31..24>	R241	FB_D_DQ4	RAM	RAM		FB_D_DQ_R<39..32>	R242	FB_D_DQ5	RAM	RAM		FB_D_DQ_R<47..40>	R243	FB_D_DQ6	RAM	RAM		FB_D_DQ_R<55..48>	R244	FB_D_DQ7	RAM	RAM		FB_D_DQ_R<63..56>			
NET_TYPE																																																																																																																																																																																																																																						
ELECTRICAL_CONSTRAINT_SET		SPACING	PHYSICAL	DIFFERENTIAL_PAIR																																																																																																																																																																																																																																		
R210		FB_D_CLK_0	RAM_DIFF	RAM_DIFF	FB_D_CLK_0_R	FB_D_CLKDDR_0_P_R																																																																																																																																																																																																																																
R211		(provided above)	RAM_DIFF	RAM_DIFF	FB_D_CLK_0_R	FB_D_CLKDDR_0_N_R																																																																																																																																																																																																																																
R212		FB_D_CLK_1	RAM_DIFF	RAM_DIFF	FB_D_CLK_1_R	FB_D_CLKDDR_1_P_R																																																																																																																																																																																																																																
R213		(provided above)	RAM_DIFF	RAM_DIFF	FB_D_CLK_1_R	FB_D_CLKDDR_1_N_R																																																																																																																																																																																																																																
R214		FB_D_ADDR_CTL	RAM	RAM		FB_D_CKE_R																																																																																																																																																																																																																																
R215		FB_D_ADDR_CTL	RAM	RAM		FB_D_CS_L_R																																																																																																																																																																																																																																
R216		FB_D_ADDR_CTL	RAM	RAM		FB_D_ADDR_R<12..0>																																																																																																																																																																																																																																
R217		FB_D_ADDR_CTL	RAM	RAM		FB_D_BA_R<2..0>																																																																																																																																																																																																																																
R218		FB_D_ADDR_CTL	RAM	RAM		FB_D_RAS_L_R																																																																																																																																																																																																																																
R219		FB_D_ADDR_CTL	RAM	RAM		FB_D_CAS_L_R																																																																																																																																																																																																																																
R220		FB_D_ADDR_CTL	RAM	RAM		FB_D_WE_L_R																																																																																																																																																																																																																																
R221		FB_D_DQS0	RAM	RAM		FB_D_DQS_R<0>																																																																																																																																																																																																																																
R222		FB_D_DQS1	RAM	RAM		FB_D_DQS_R<1>																																																																																																																																																																																																																																
R223		FB_D_DQS2	RAM	RAM		FB_D_DQS_R<2>																																																																																																																																																																																																																																
R224		FB_D_DQS3	RAM	RAM		FB_D_DQS_R<3>																																																																																																																																																																																																																																
R225		FB_D_DQS4	RAM	RAM		FB_D_DQS_R<4>																																																																																																																																																																																																																																
R226		FB_D_DQS5	RAM	RAM		FB_D_DQS_R<5>																																																																																																																																																																																																																																
R227		FB_D_DQS6	RAM	RAM		FB_D_DQS_R<6>																																																																																																																																																																																																																																
R228		FB_D_DQS7	RAM	RAM		FB_D_DQS_R<7>																																																																																																																																																																																																																																
R229		FB_D_DQM0	RAM	RAM		FB_D_DQM_R<0>																																																																																																																																																																																																																																
R230		FB_D_DQM1	RAM	RAM		FB_D_DQM_R<1>																																																																																																																																																																																																																																
R231		FB_D_DQM2	RAM	RAM		FB_D_DQM_R<2>																																																																																																																																																																																																																																
R232		FB_D_DQM3	RAM	RAM		FB_D_DQM_R<3>																																																																																																																																																																																																																																
R233		FB_D_DQM4	RAM	RAM		FB_D_DQM_R<4>																																																																																																																																																																																																																																
R234		FB_D_DQM5	RAM	RAM		FB_D_DQM_R<5>																																																																																																																																																																																																																																
R235		FB_D_DQM6	RAM	RAM		FB_D_DQM_R<6>																																																																																																																																																																																																																																
R236		FB_D_DQM7	RAM	RAM		FB_D_DQM_R<7>																																																																																																																																																																																																																																
R237		FB_D_DQ0	RAM	RAM		FB_D_DQ_R<7..0>																																																																																																																																																																																																																																
R238		FB_D_DQ1	RAM	RAM		FB_D_DQ_R<15..8>																																																																																																																																																																																																																																
R239		FB_D_DQ2	RAM	RAM		FB_D_DQ_R<23..16>																																																																																																																																																																																																																																
R240		FB_D_DQ3	RAM	RAM		FB_D_DQ_R<31..24>																																																																																																																																																																																																																																
R241		FB_D_DQ4	RAM	RAM		FB_D_DQ_R<39..32>																																																																																																																																																																																																																																
R242		FB_D_DQ5	RAM	RAM		FB_D_DQ_R<47..40>																																																																																																																																																																																																																																
R243		FB_D_DQ6	RAM	RAM		FB_D_DQ_R<55..48>																																																																																																																																																																																																																																
R244		FB_D_DQ7	RAM	RAM		FB_D_DQ_R<63..56>																																																																																																																																																																																																																																
												<table><tr><td colspan="3">M11 Frame Buffer Constraints</td></tr><tr><td colspan="3">SYNC_MASTER=N/A</td><td colspan="3">SYNC_DATE=N/A</td></tr><tr><td colspan="6">NOTICE OF PROPRIETARY PROPERTY</td></tr><tr><td colspan="6">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</td></tr><tr><td colspan="6">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</td></tr><tr><td colspan="6">II NOT TO REPRODUCE OR COPY IT</td></tr><tr><td colspan="6">III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</td></tr></table>				M11 Frame Buffer Constraints			SYNC_MASTER=N/A			SYNC_DATE=N/A			NOTICE OF PROPRIETARY PROPERTY						THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING						I TO MAINTAIN THE DOCUMENT IN CONFIDENCE						II NOT TO REPRODUCE OR COPY IT						III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART																																																																																																																																																																																					
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8		7		6		5		4		3		2		1																																																																																																																																																																																																																								



Page Notes

Power aliases required by this page:

- =PP3V3_AGP
- =PP1V5_AGP
- =PP1V5_I2_AGP

Signal aliases required by this page:

- =I2_AGP_VREF - VRef from graphics card or on-board graphics controller
- =I2_AGP_FBCLK_IN - AGP feedback clock input. Length should match that of clock from I2 to AGP device.

BOM options provided by this page:

(NONE)

NOTE: I2 implements an AGP 4x bridge. AGP 8x signals are not provided by this page.

I2 AGP Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

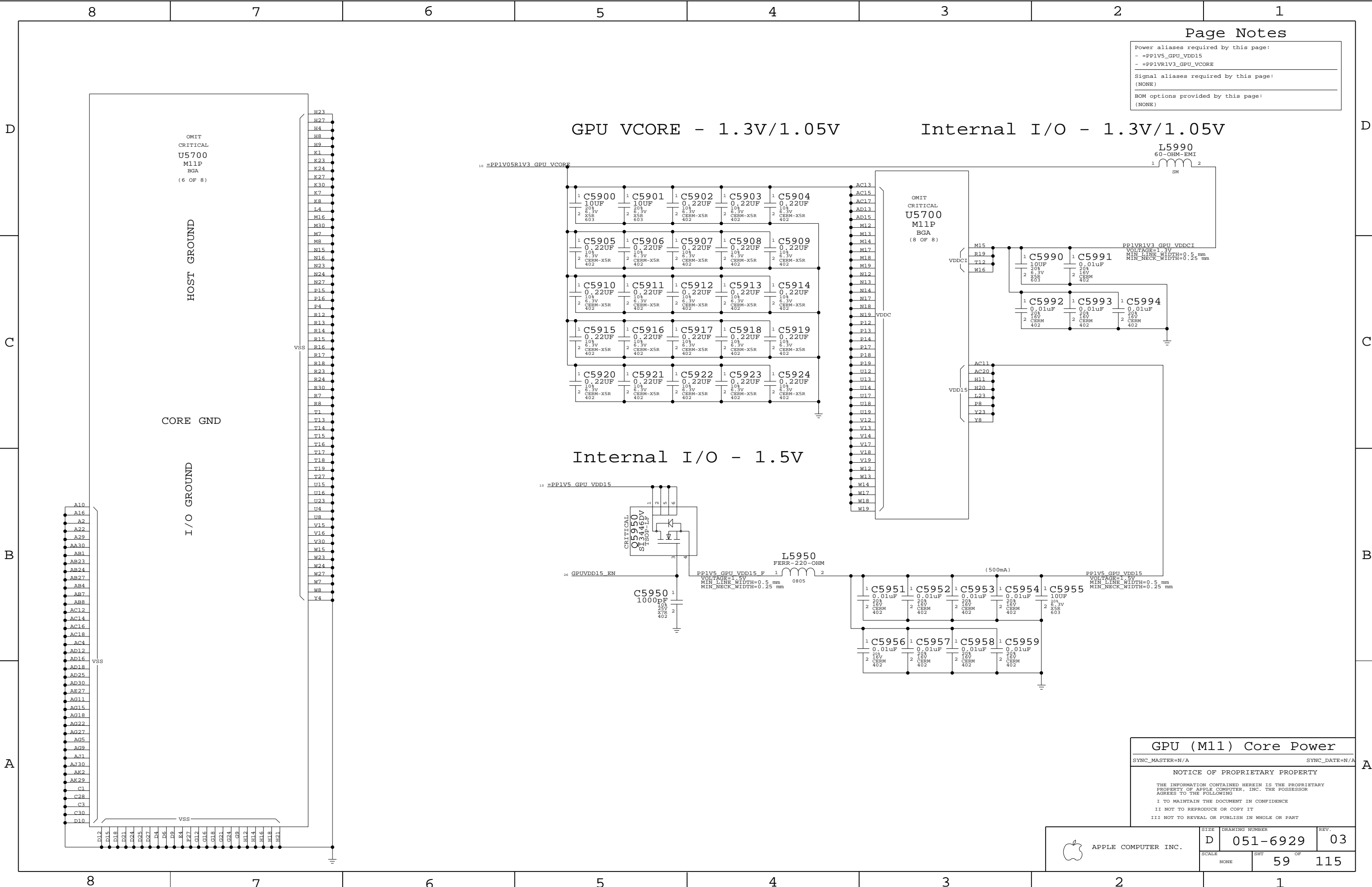
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Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GPU Vcore - 1.3V/1.05V

Internal I/O - 1.3V/1.05V

Internal I/O - 1.5V

GPU (M11) Core Power

SYNC_MASTER=N/A SYNC_DATE=N/A

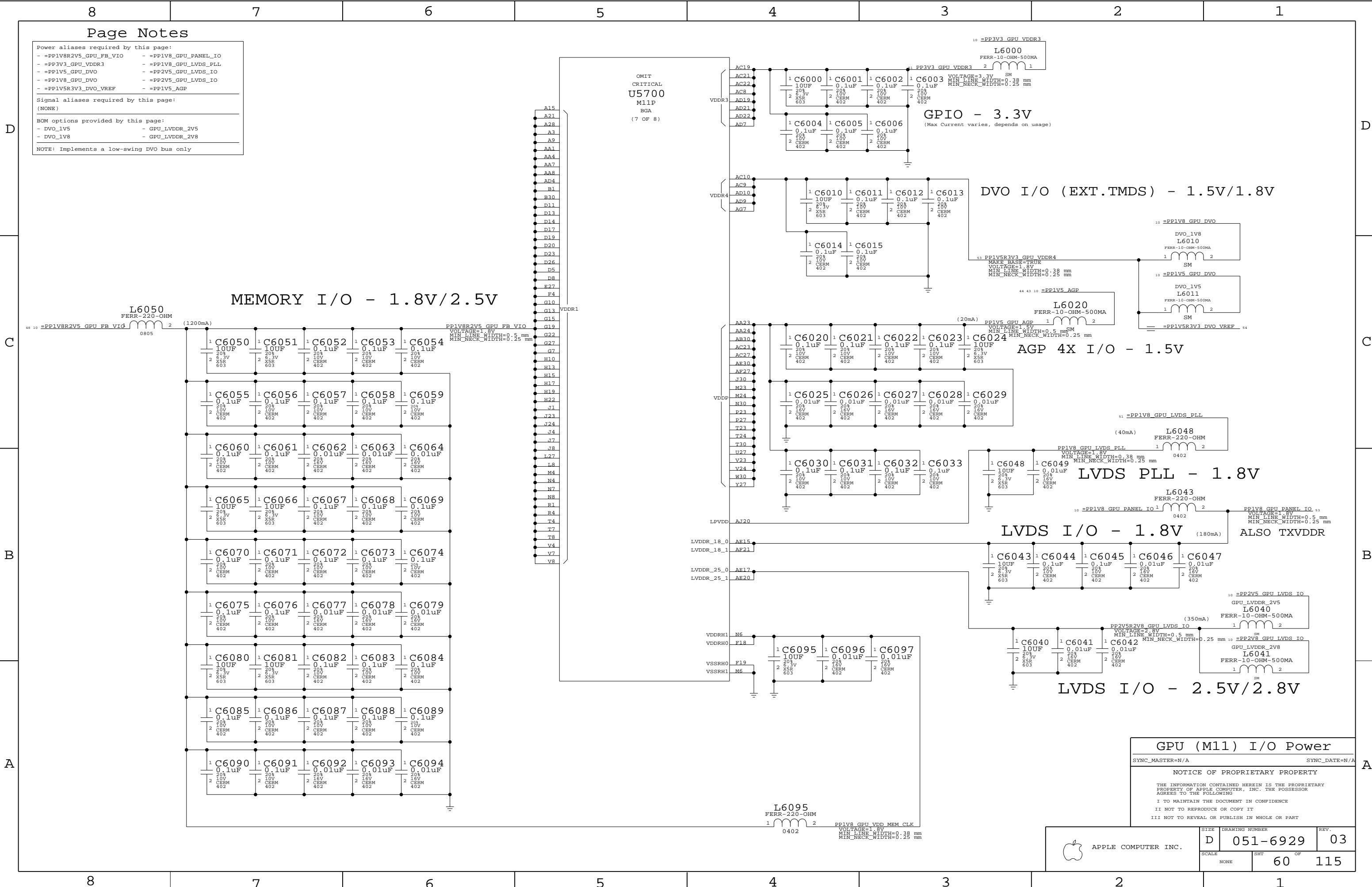
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SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	59	115



8

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Page Notes

Power aliases required by this page:

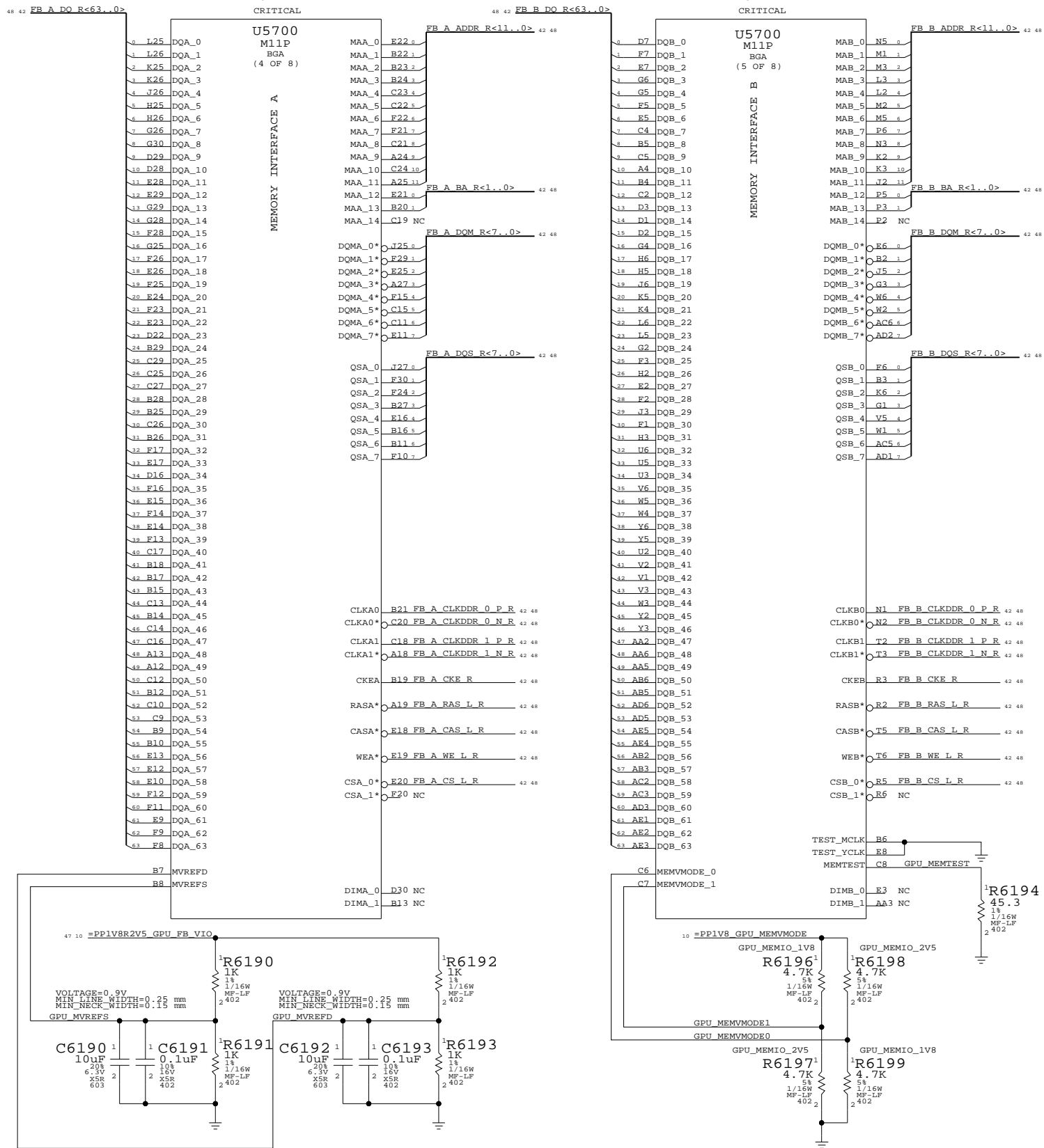
- =PP1V8R2V5_GPU_FB_VIO
- =PP1V8_GPU_MEMVMODE

Signal aliases required by this page:

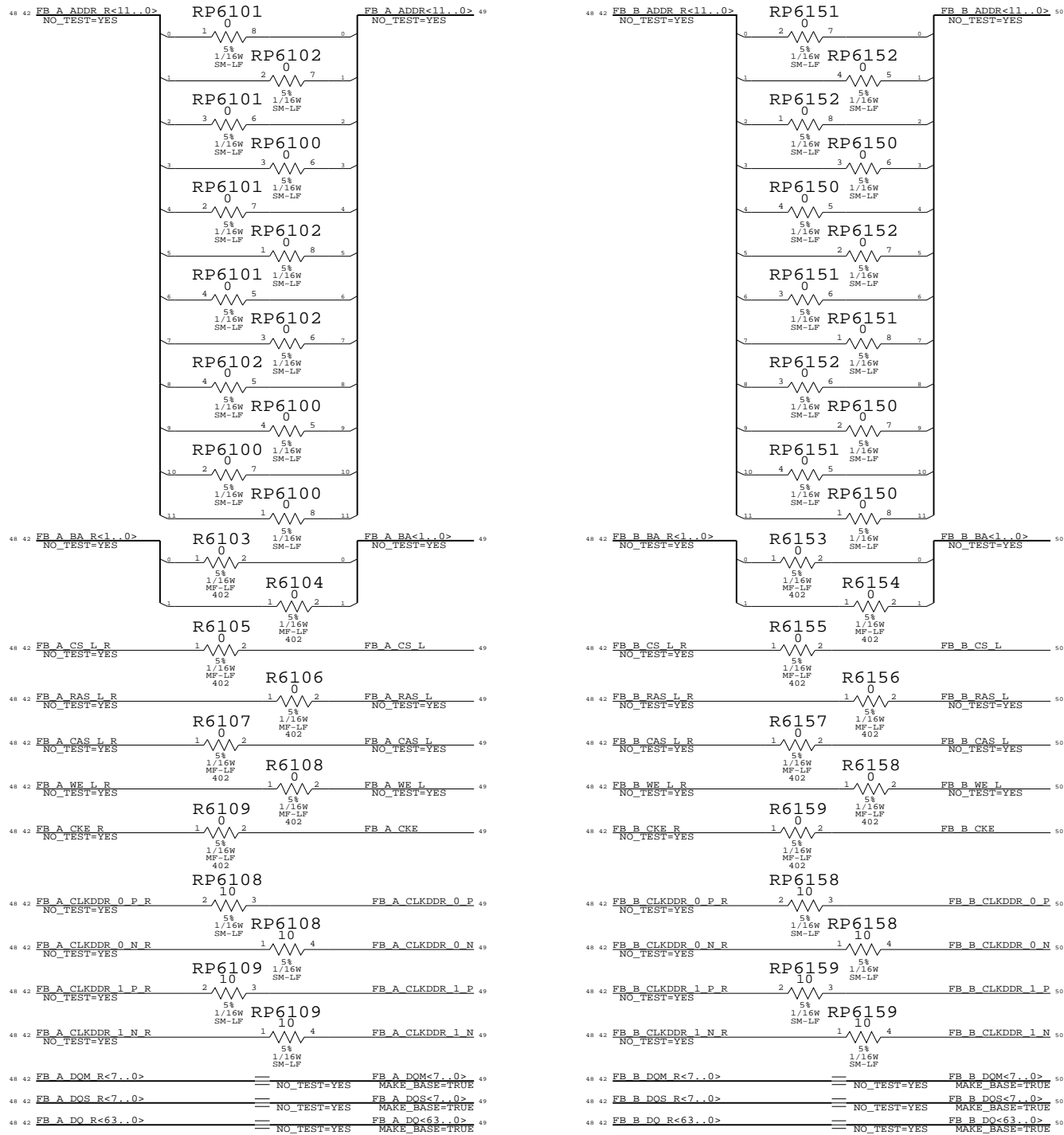
(NONE)

BOM options provided by this page:

- GPU_MEMIO_1V8
- GPU_MEMIO_2V5



GPU Frame Buffer Series Term



GPU (M11) Frame Buffer I/F

SYNC_MASTER=N/A SYNC_DATE=N/A

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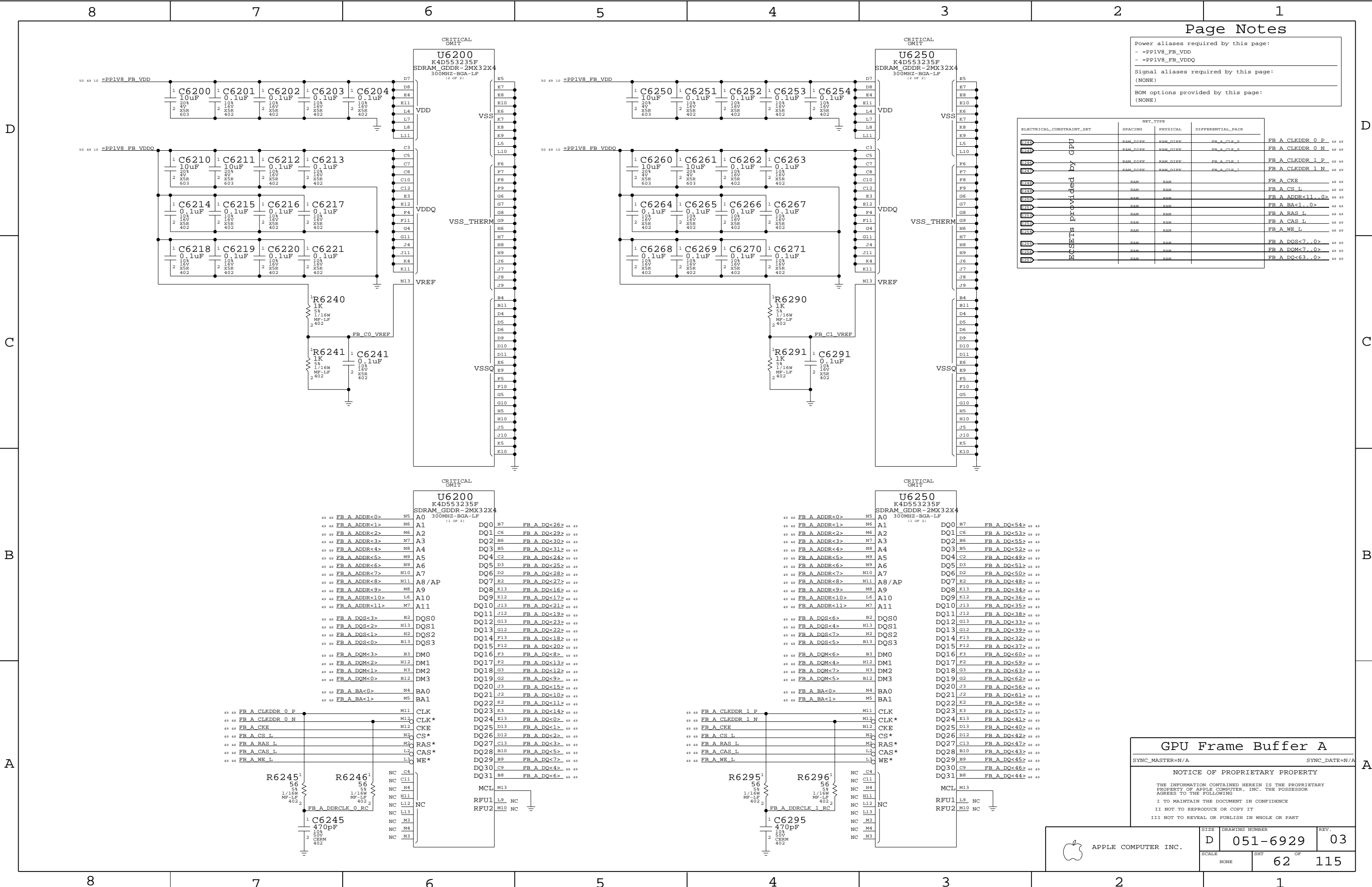
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SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	61	115



Page Notes

Power aliases required by this page:

- =PPIV8_FB_VDD
- =PPIV8_FB_VDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
RESETS Provided by GPU	RAM_DIFF	RAM_DIFF	FB_A_CLK_0	FB A CLKDDR 0 P 48 49
	RAM_DIFF	RAM_DIFF	FB_A_CLK_0	FB A CLKDDR 0 N 48 49
	RAM_DIFF	RAM_DIFF	FB_A_CLK_1	FB A CLKDDR 1 P 48 49
	RAM_DIFF	RAM_DIFF	FB_A_CLK_1	FB A CLKDDR 1 N 48 49
	RAM	RAM	FB_A_CKE	FB A CKE 48 49
	RAM	RAM	FB_A_CS_L	FB A CS_L 48 49
	RAM	RAM	FB_A_ADDR<11..0>	FB A ADDR<11..0> 48 49
	RAM	RAM	FB_A_BA<1..0>	FB A BA<1..0> 48 49
	RAM	RAM	FB_A_RAS_L	FB A RAS_L 48 49
	RAM	RAM	FB_A_CAS_L	FB A CAS_L 48 49
	RAM	RAM	FB_A_WE_L	FB A WE_L 48 49
	RAM	RAM	FB_A_DQS<7..0>	FB A DQS<7..0> 48 49
	RAM	RAM	FB_A_DQM<7..0>	FB A DQM<7..0> 48 49
	RAM	RAM	FB_A_DQ<63..0>	FB A DQ<63..0> 48 49
	RAM	RAM	FB_A_DQ<63..0>	FB A DQ<63..0> 48 49
	RAM	RAM	FB_A_DQ<63..0>	FB A DQ<63..0> 48 49

GPU Frame Buffer A

SYNC_MASTER=N/A SYNC_DATE=N/A

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Power aliases required by this page:
- =PPIV8_FB_VDD
- =PPIV8_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
RESETS Provided by GPU	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_A	FB_B_CLKDDR_0_P 48 50
	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_N	FB_B_CLKDDR_0_N 48 50
	RAM_DIFF	RAM_DIFF	FB_B_CLK_1	FB_B_CLKDDR_1_P 48 50
	RAM_DIFF	RAM_DIFF	FB_B_CLK_1	FB_B_CLKDDR_1_N 48 50
	RAM	RAM		FB_B_CKE 48 50
	RAM	RAM		FB_B_CS_L 48 50
	RAM	RAM		FB_B_ADDR<11..0> 48 50
	RAM	RAM		FB_B_BA<1..0> 48 50
	RAM	RAM		FB_B_RAS_L 48 50
	RAM	RAM		FB_B_CAS_L 48 50
	RAM	RAM		FB_B_WE_L 48 50
	RAM	RAM		FB_B_DQS<7..0> 48 50
	RAM	RAM		FB_B_DOM<7..0> 48 50
	RAM	RAM		FB_B_DQ<63..0> 48 50
	RAM	RAM		
	RAM	RAM		

GPU Frame Buffer B

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	63	115

8

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Page Notes

Power aliases required by this page:

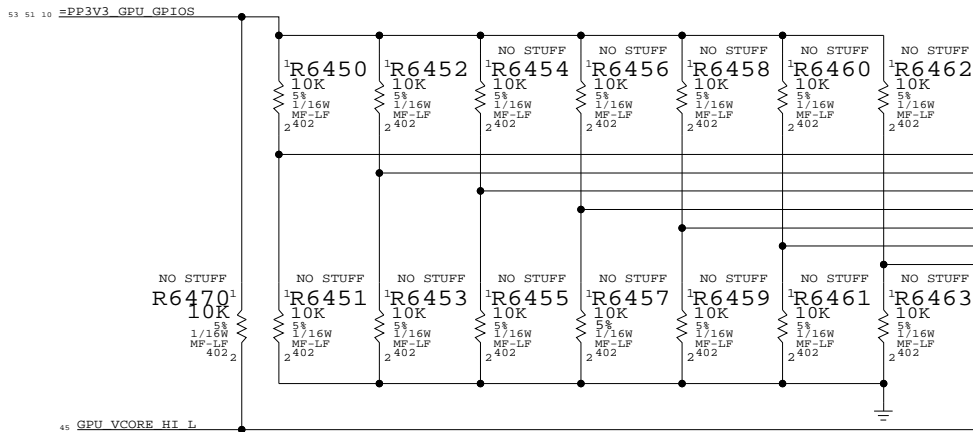
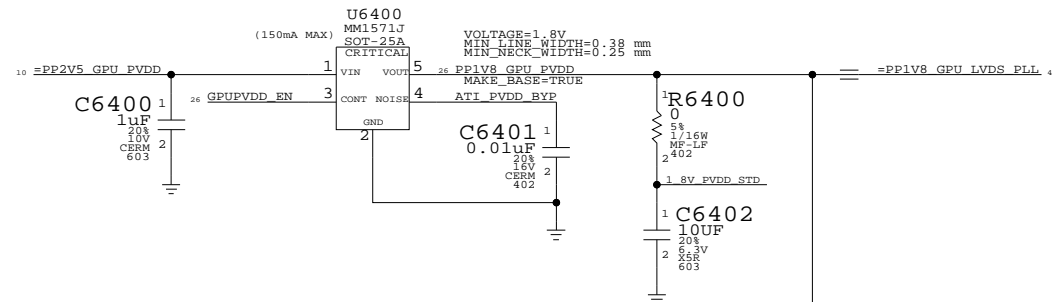
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:

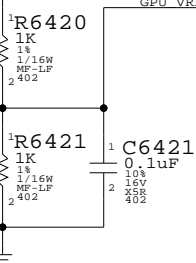
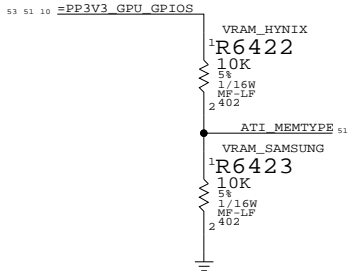
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:

(NONE)



ATI AGP FBSKEW<0>	AJ5	GPIO_0
ATI AGP FBSKEW<1>	AH5	GPIO_1
ATI X1CLK SKREW<0>	AJ4	GPIO_2
ATI X1CLK SKREW<1>	AH4	GPIO_3
ATI BUS CFG<0>	AH4	GPIO_4
ATI BUS CFG<1>	AF4	GPIO_5
ATI BUS CFG<2>	AJ3	GPIO_6
TP EXTIMDS RESET L	AJ3	GPIO_7
TP ATI GPIO8	AH3	GPIO_8
TP ATI GPIO9	AJ2	GPIO_9
TP ATI GPIO10	AH2	GPIO_10
TP ATI GPIO11	AH1	GPIO_11
TP ATI GPIO12	AG3	GPIO_12
ATI MEMTYPE	AG1	GPIO_13
HPD_PWR SNS_EN	AG2	GPIO_14
ATI CLK27M_SS	AF3	GPIO_15
	AF2	GPIO_16



GPU (M11) GPIOs/Straps

SYNC_MASTER=N/A

SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	64	115

Page Notes

Power aliases required by this page:

- =PP3V3_GPU_CLOCKS
- =PP3V3_GPU_PWRSEQ
- =PPVIN_GPU_LVDDR_LDO
- =PP2V5_GPU_PWRSEQ
- =PP2V5_GPU_LVDDR_LDO
- =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

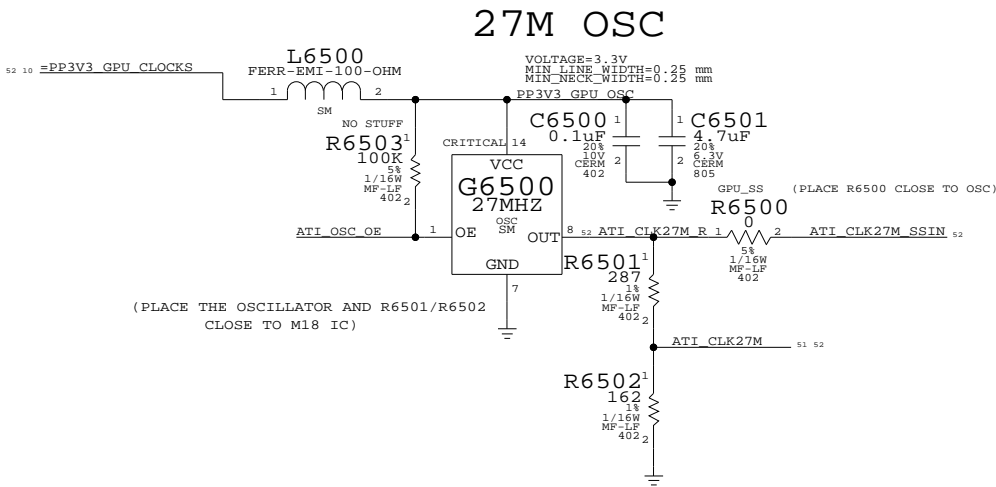
Signal aliases required by this page:

(NONE)

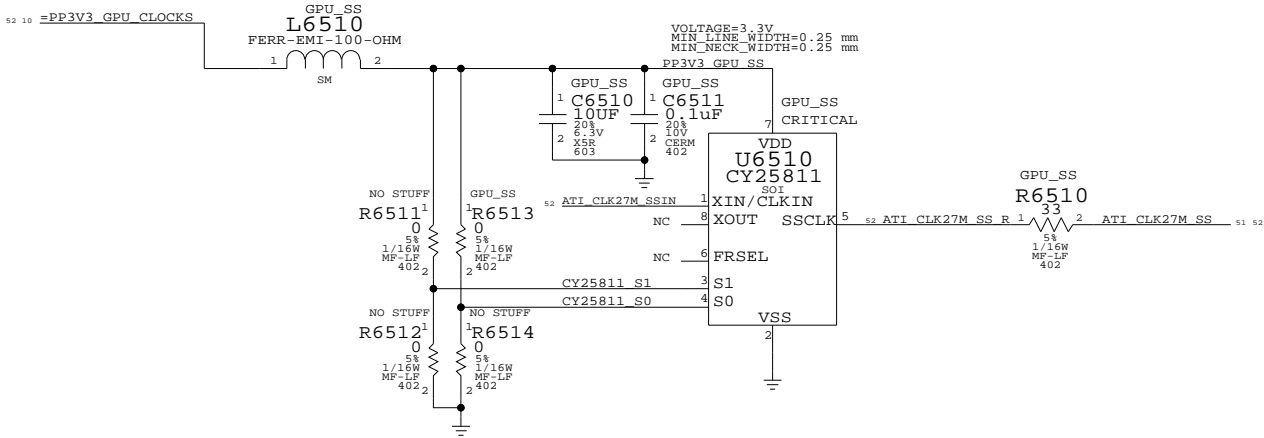
BOM options provided by this page:

- GPU_SS
- GPU_LVDDR_2V8

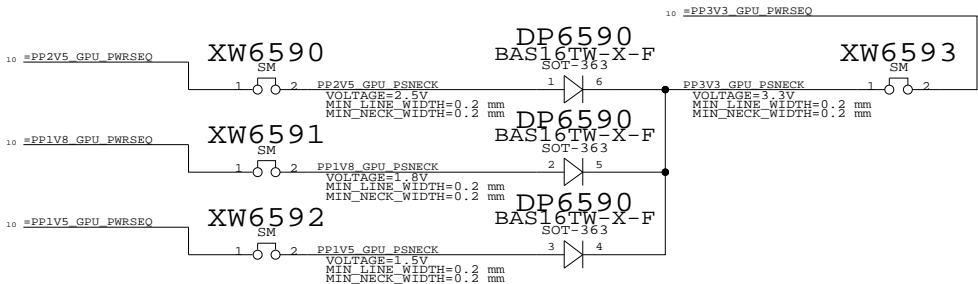
NET_TYPE					
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
R650	ATI_CLK27M	CLOCK	CLOCK	ATI_CLK27M_R	52
R64	ATI_CLK27M	CLOCK	CLOCK	ATI_CLK27M	51 52
R65	ATI_CLK27M	CLOCK	CLOCK	ATI_CLK27M_SSIN	52
R61	ATI_CLK27M_SS	CLOCK	CLOCK	ATI_CLK27M_SS_R	52
R62	ATI_CLK27M_SS	CLOCK	CLOCK	ATI_CLK27M_SS	51 52



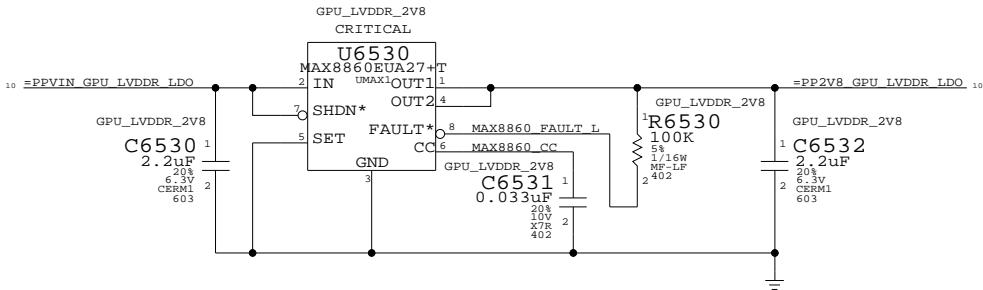
SPREAD SPECTRUM SUPPORT
S0=1;S1=M => -1.5% DOWN-SPREAD



M11 Power Shutdown Sequencing



LVDDR 2.8V LDO



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35380647	35381140	GPU_LVDDR_2V8	U6530	2.82V instead of 2.77V

GPU (M11) Clocks/Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	65	115

D

C

B

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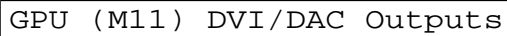
1

D

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SYNC_MASTER=N/A	SYNC_DATE=N/A
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SIZE	DRAWING NUMBER
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D	051-6929
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REV.

03

SCALE	

SHT

8	7	6	5	4	3	2	1
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D

NOTE: Target differential impedance for
TMDs data pairs is 100 ohms.

C

B



5



TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN

B

	SIZE	DRAWING NUMBER
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 λ

Page Notes

Power aliases required by this page:
- =PP3V3_RUN_SI

Signal aliases required by this page:
- =SI_I2C_CLK - =SI_TMDS_RESET_L
- =SI_I2C_DATA - =RP68xxPy (pinswappable series R)

BOM options provided by this page:
- TMDS_DUAL

Net Spacing Type: TMDS

Net Physical Type: TMDS

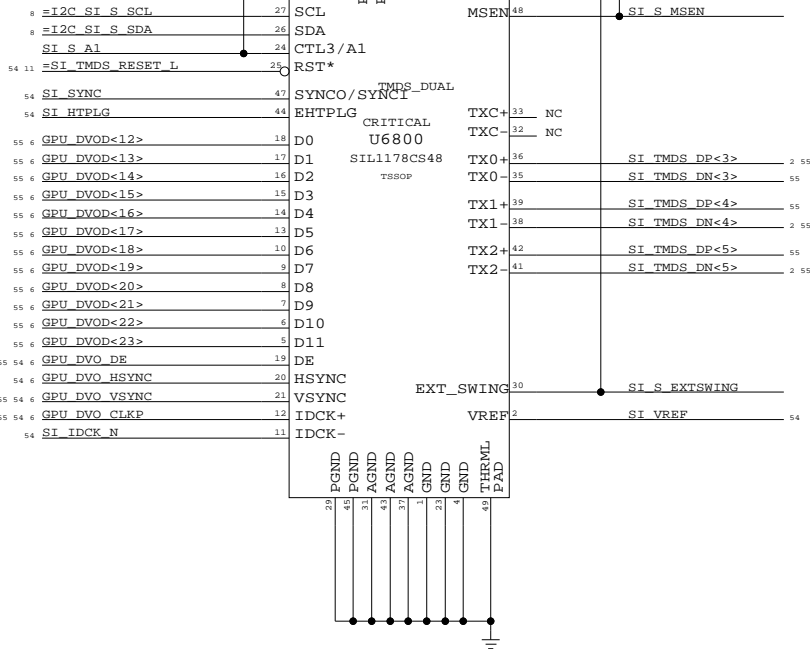
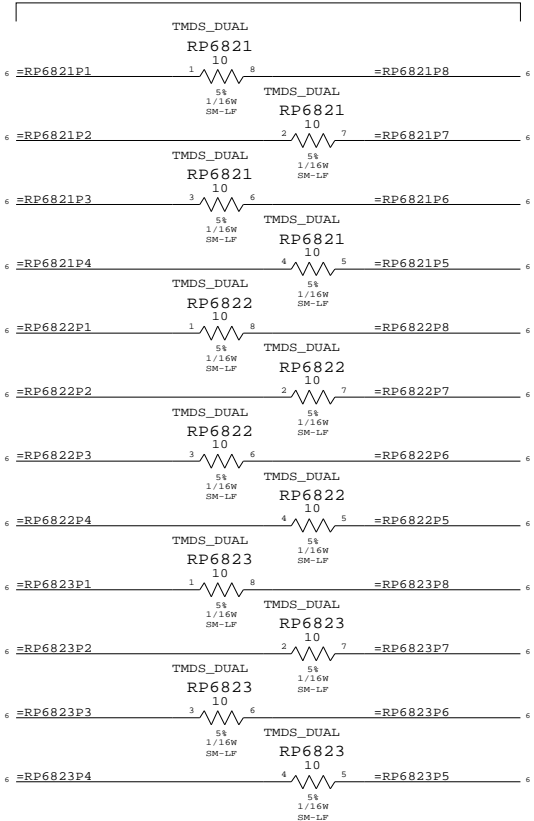
NOTE: Target differential impedance for
TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
GPU_DVO_UPPER	DVO	DVO	GPU_DVOD<12..19>
GPU_DVOD20	DVO	DVO	GPU_DVOD<20>
GPU_DVO_UPPER	DVO	DVO	GPU_DVOD<21..23>
PROVIDED BY LOWER TMR			GPU_DVO_VSYNC
PROVIDED BY LOWER TMR			GPU_DVO_DE
PROVIDED BY LOWER TMR			GPU_DVO_CLKP
TMDS_DATA	TMDS	TMDS	SI_TMDS_D3
TMDS_DATA	TMDS	TMDS	SI_TMDS_D3
TMDS_DATA	TMDS	TMDS	SI_TMDS_D4
TMDS_DATA	TMDS	TMDS	SI_TMDS_D4
TMDS_DATA	TMDS	TMDS	SI_TMDS_D5
TMDS_DATA	TMDS	TMDS	SI_TMDS_D5
TMDS_D3	TMDS	TMDS	TMDS_D3
TMDS_D3	TMDS	TMDS	TMDS_D3
TMDS_D4	TMDS	TMDS	TMDS_D4
TMDS_D4	TMDS	TMDS	TMDS_D4
TMDS_D5	TMDS	TMDS	TMDS_D5
TMDS_D5	TMDS	TMDS	TMDS_D5

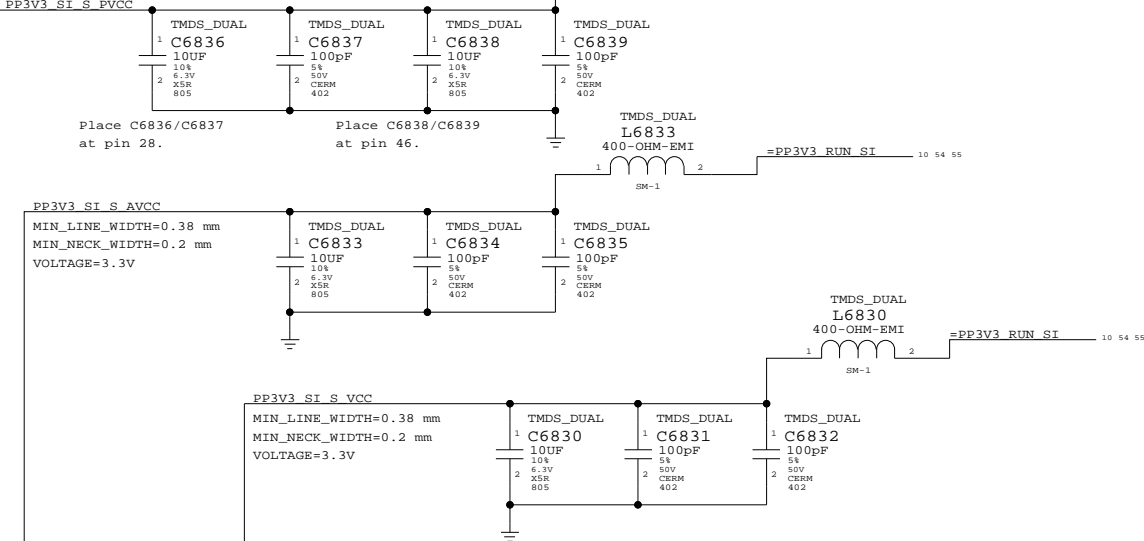
Upper DVO series termination

Place close to GPU

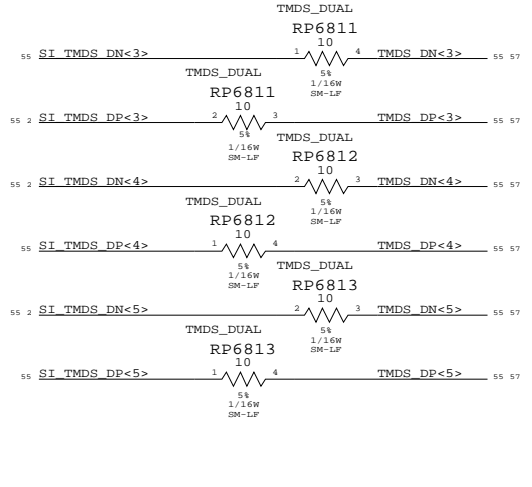
One for each of: GPU_DVOD<12..23>



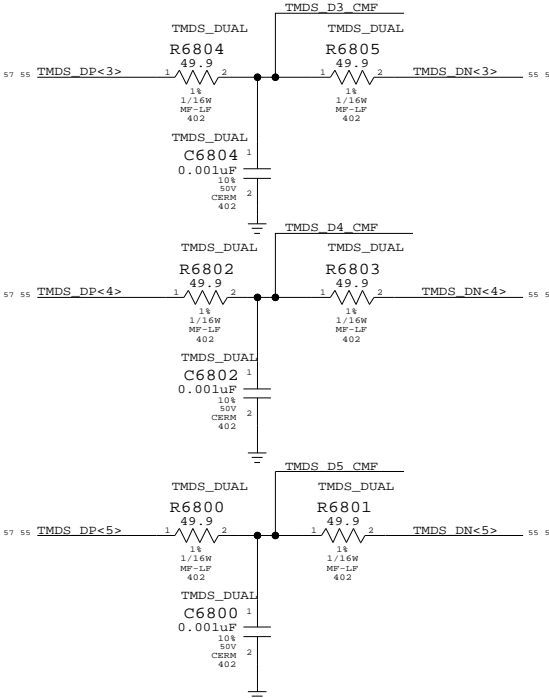
VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.38 mm
PP3V3_SI_S_PVCC



Upper Channel Series Termination



Upper Channel Common-mode Termination



Upper TMDS Transmitter

SYNC_MASTER=N/A SYNC_DATE=N/A

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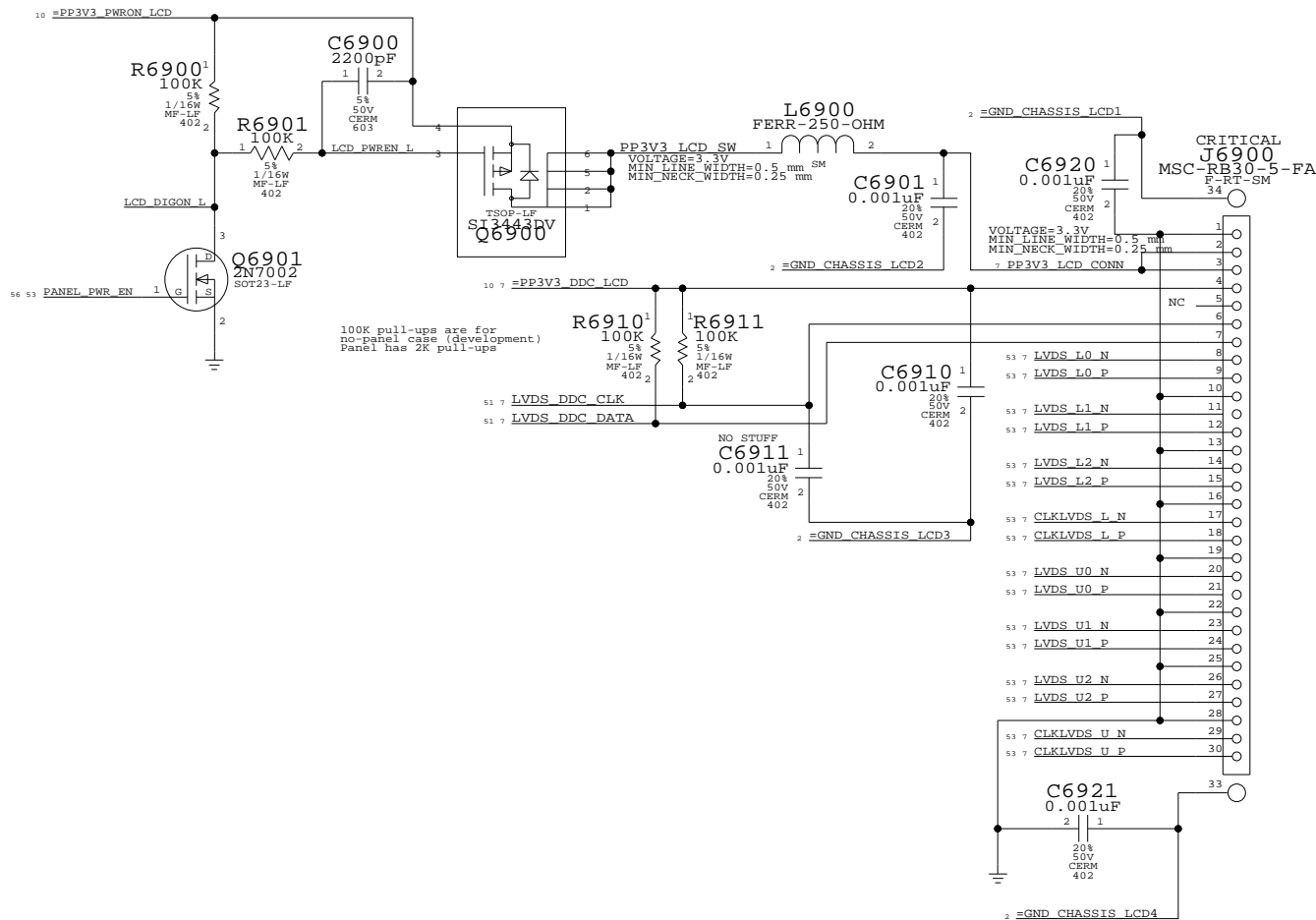
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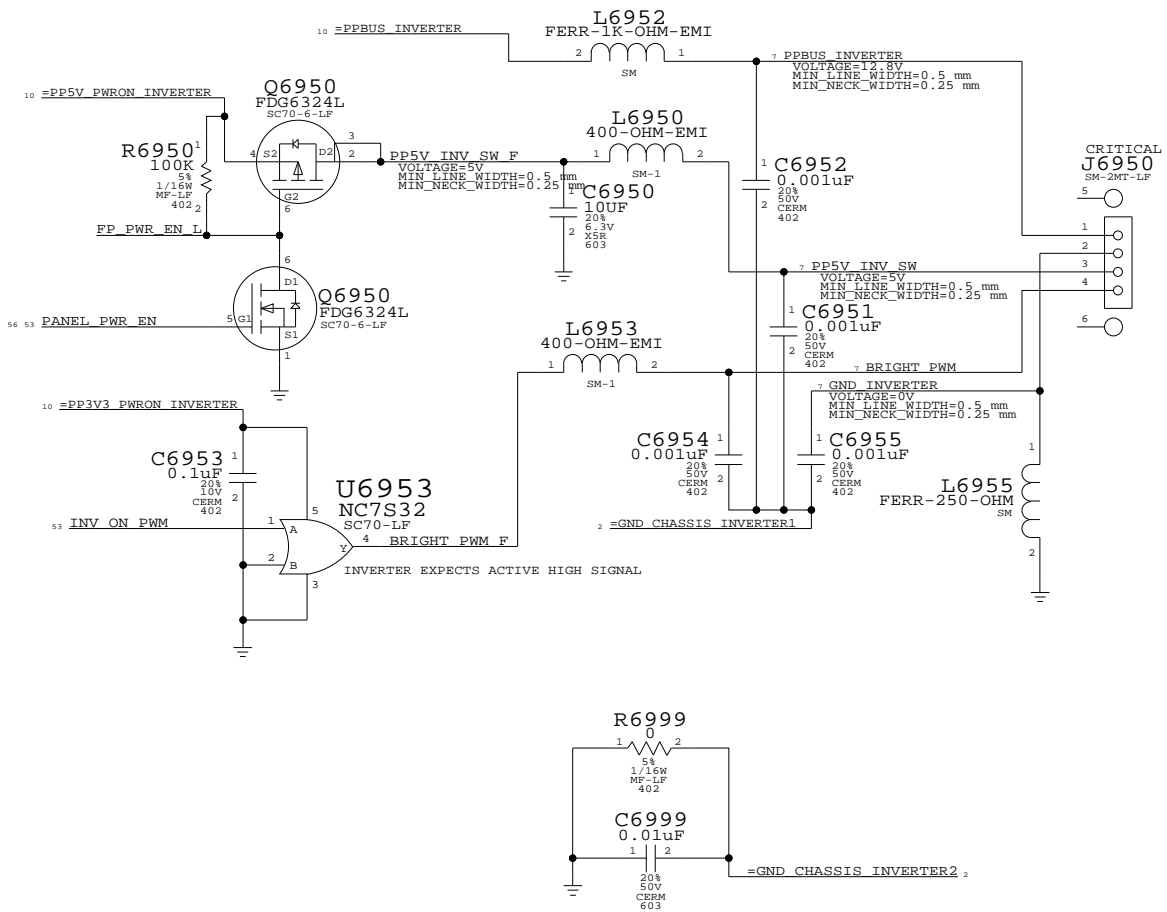
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SCALE	NONE	SHT	68	OF	115

LCD (LVDS) INTERFACE



INVERTER INTERFACE



Internal Display Conns

SYNC_MASTER=N/A SYNC_DATE=N/A

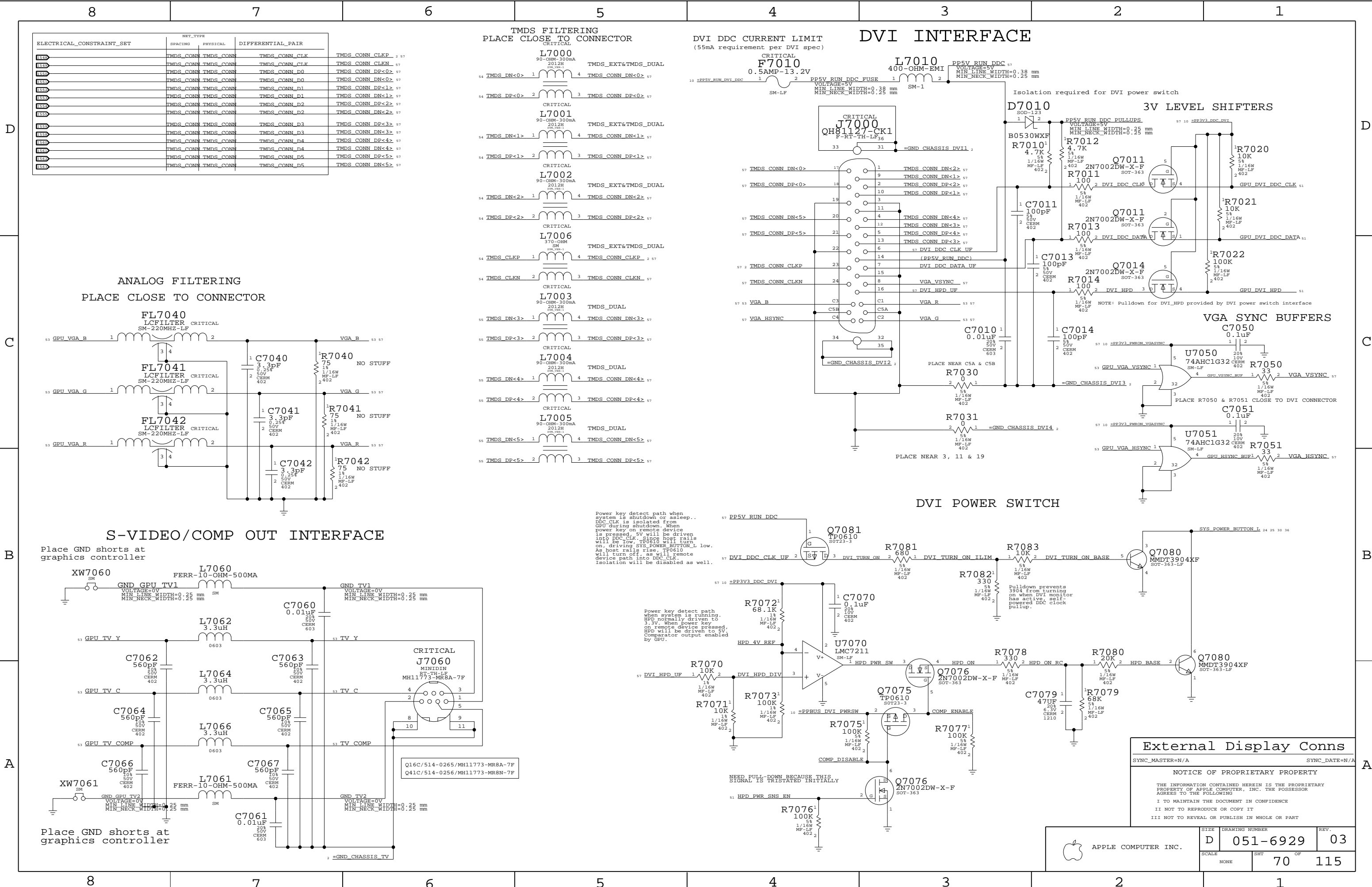
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D

C

B

A




C

B

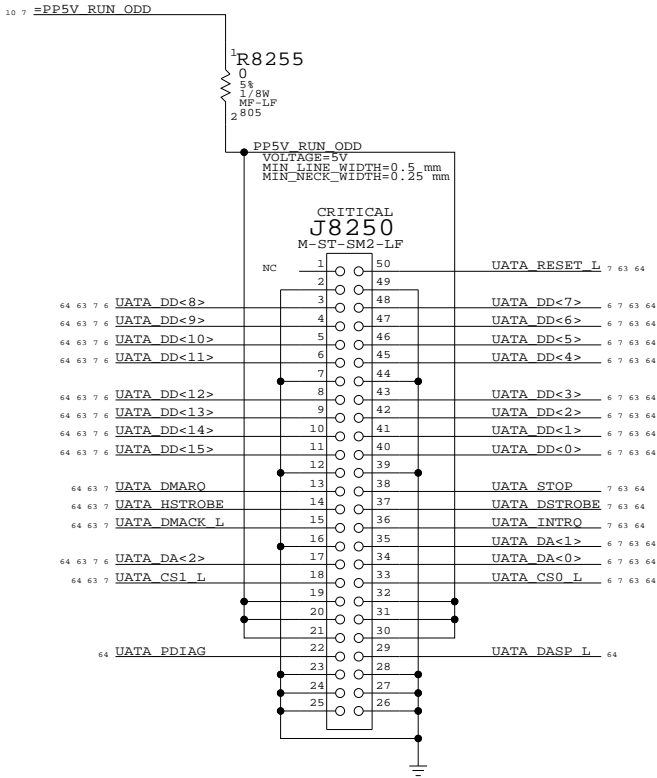
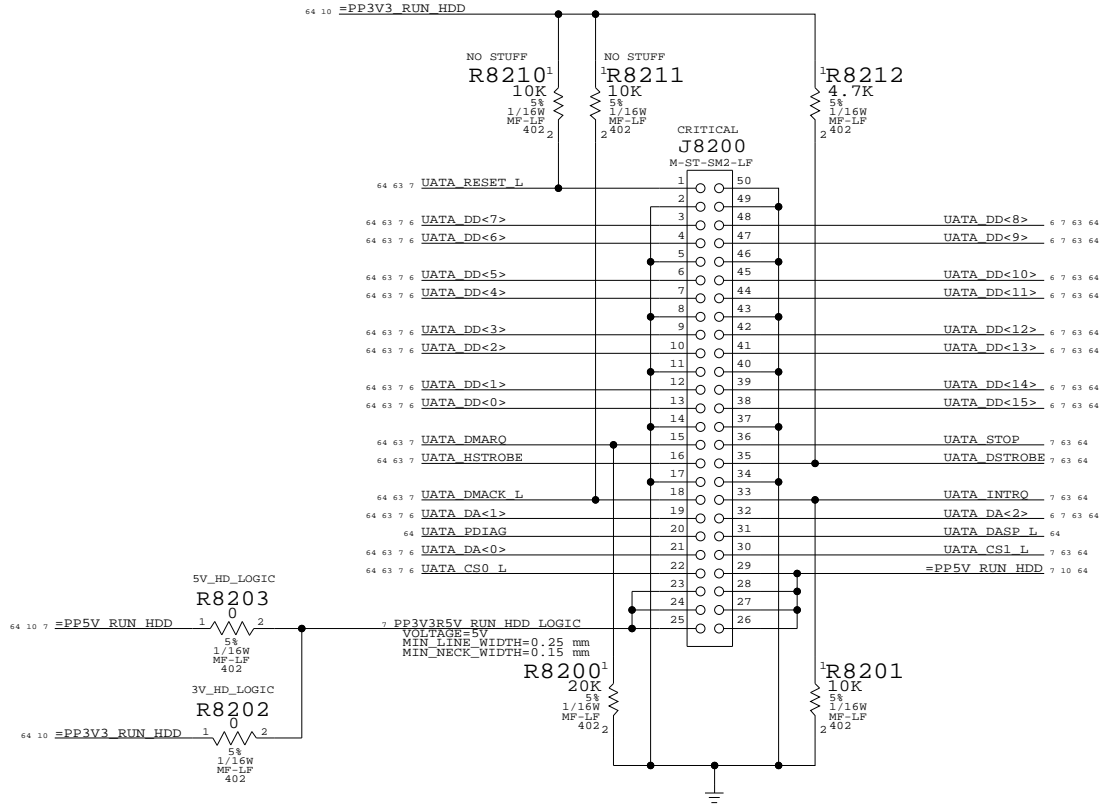
A

BootROM	
SYNC_MASTER=N/A	SYNC_DATE=N/A
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	NONE	71	115

HDD CONNECTOR

ODD CONNECTOR



ATA Connectors
Q16C/516S0357/M-ST-SM2-LF
Q41C/516S0335/M-ST-SM1-LF

HDD/ODD Connectors

SYNC_MASTER=N/A

SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

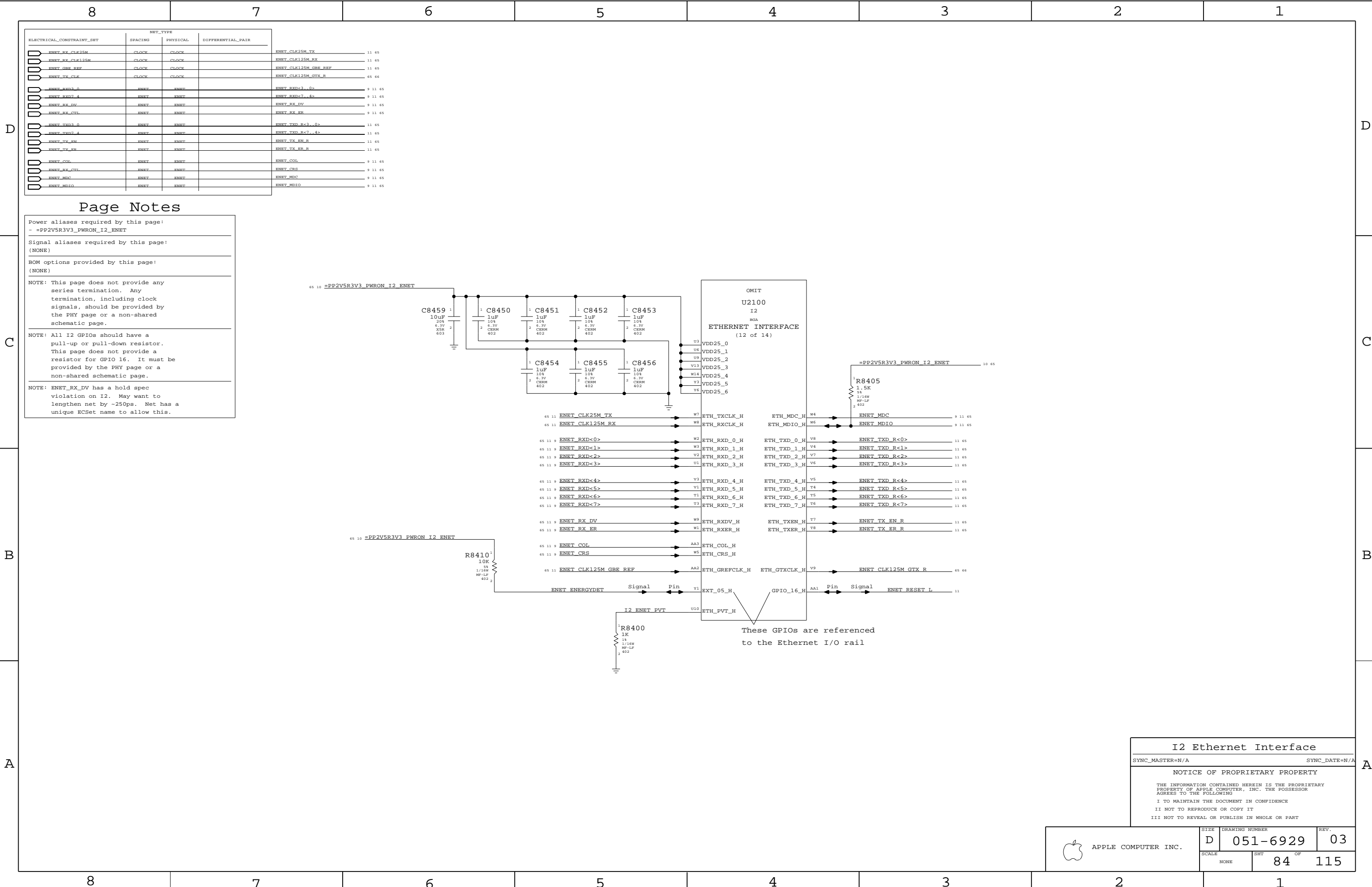
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NONE		82	115



I2 Ethernet Interface

SYNC_MASTER=N/A

SYNC_DATE=N/A

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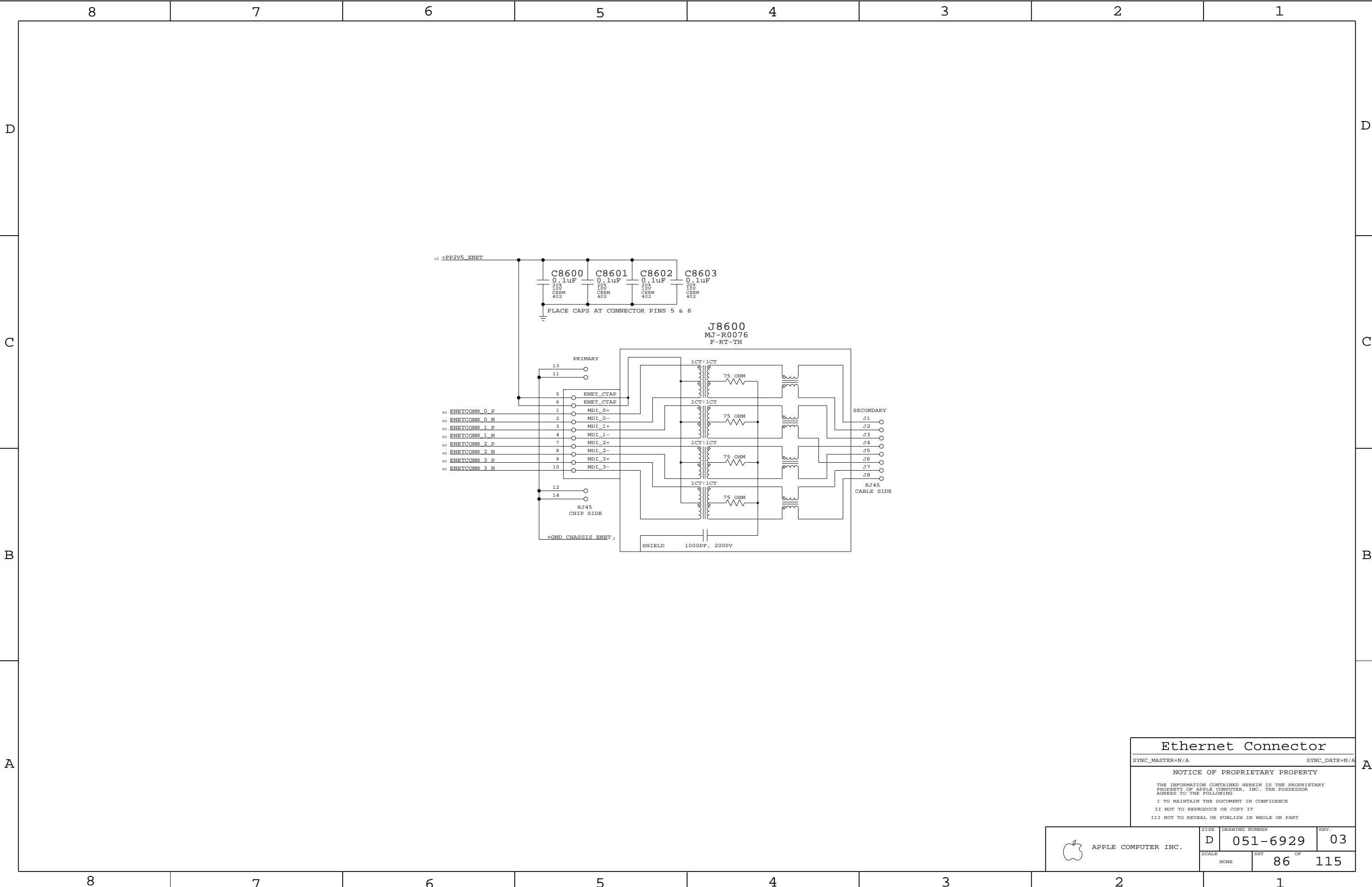
NONE

SHT

84

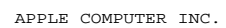
OF

115

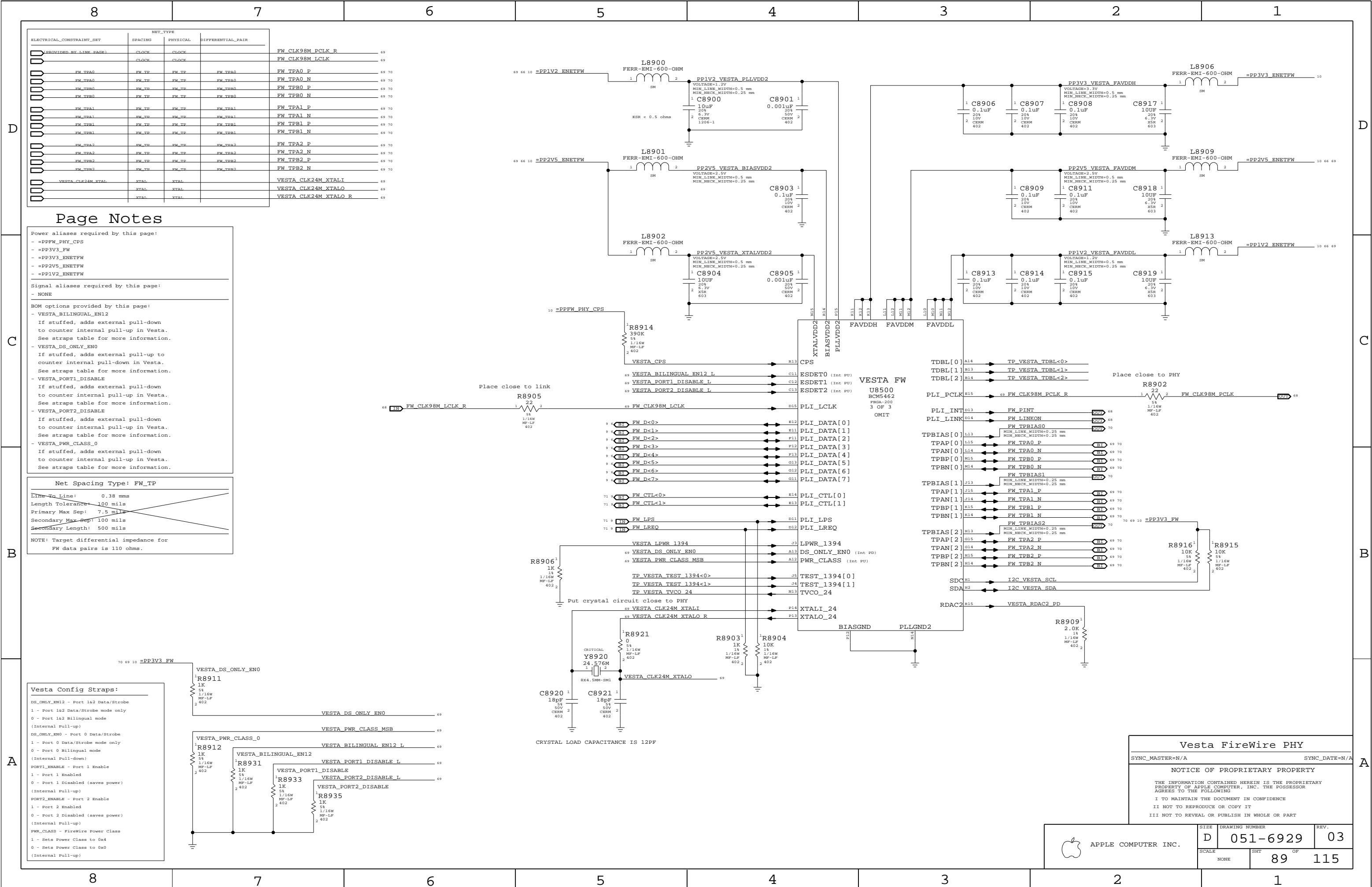


SYNC_MASTER=N/A SYNC_DATE=N/A

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
PROVIDED	FW	FW	FW_PORT1_TPA_FL	FW_PORT1_TPA_P_FL 70
	FW	FW	FW_PORT1_TPA_N_FL	FW_PORT1_TPA_N_FL 70
BY	FW	FW	FW_PORT1_TPB_FL	FW_PORT1_TPB_P_FL 70
	FW	FW	FW_PORT1_TPB_N_FL	FW_PORT1_TPB_N_FL 70
PHY	FW	FW	FW_PORT2_TPA_FL	FW_PORT2_TPA_P_FL 70
	FW	FW	FW_PORT2_TPA_N_FL	FW_PORT2_TPA_N_FL 70
PAGE	FW	FW	FW_PORT2_TPB_FL	FW_PORT2_TPB_P_FL 70
	FW	FW	FW_PORT2_TPB_N_FL	FW_PORT2_TPB_N_FL 70

Page Notes

Power aliases required by this page:

- _PPFW_PORT1
- _PPFW_PORT2
- _PPFW_PORT3
- _PP3V3_FW
- _GND_CHASSIS_FW_PORT1
- _GND_CHASSIS_FW_PORT2
- _GND_CHASSIS_FW_PORT3

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

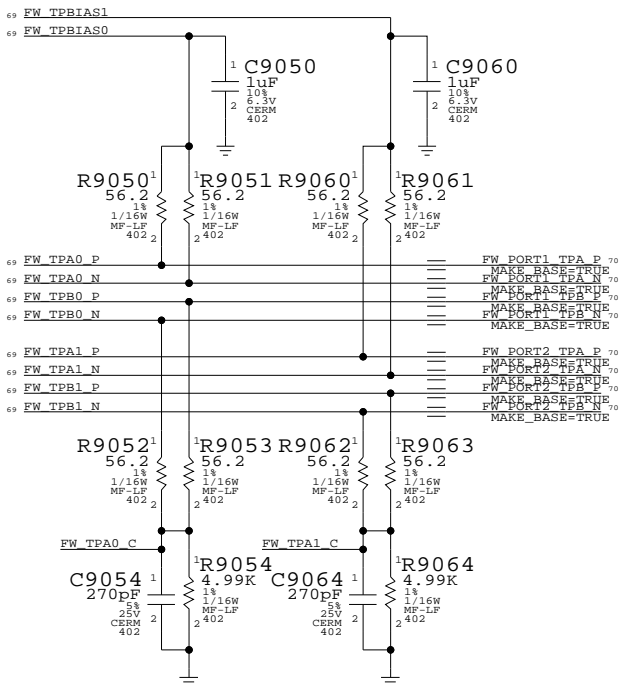
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

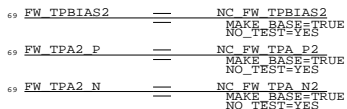
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

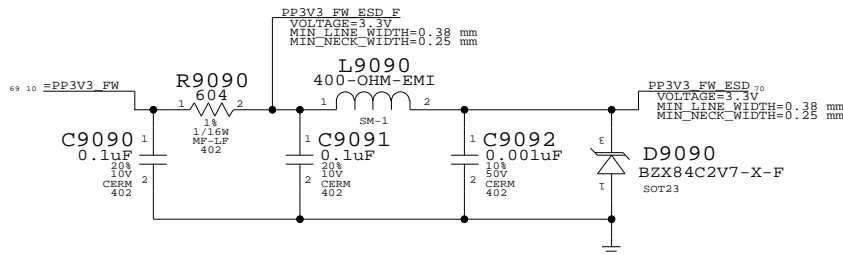
Place close to FireWire PHY



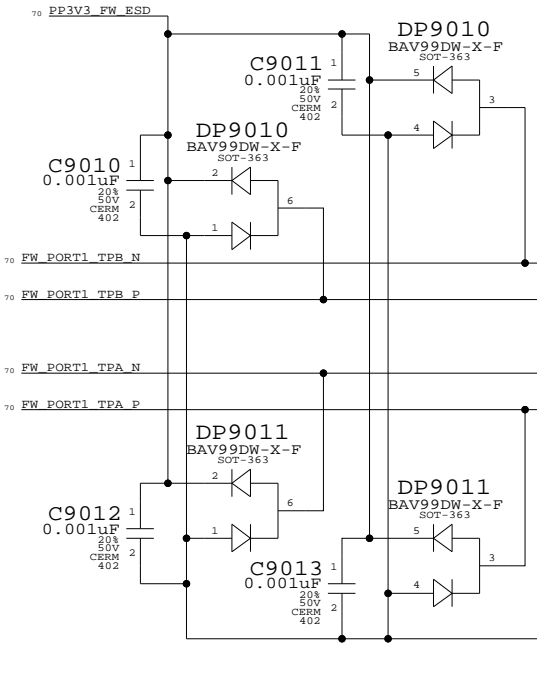
3rd TPA/TPB pair unused



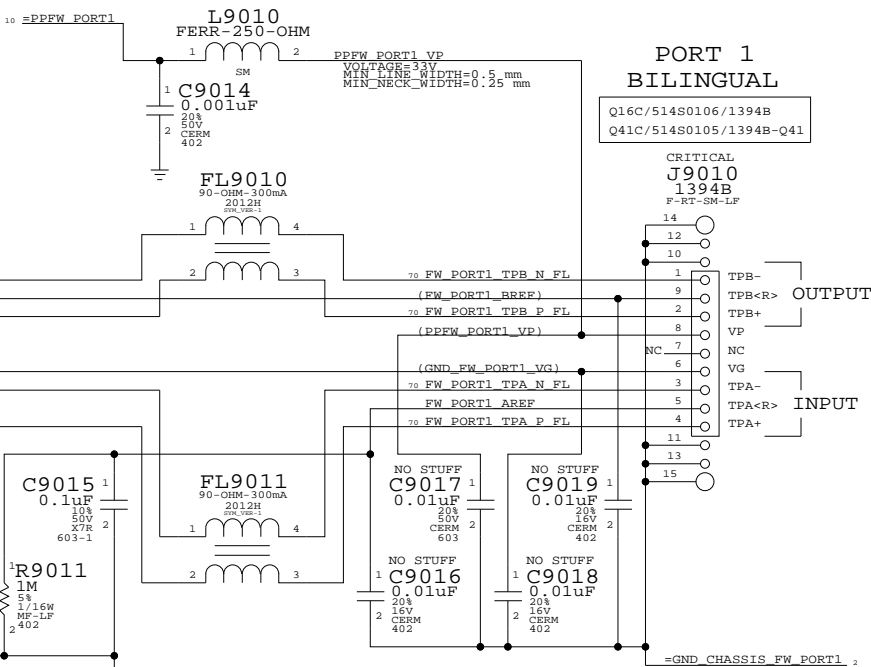
ESD Rail



"Snapback" & "Late VG" Protection



Cable Power

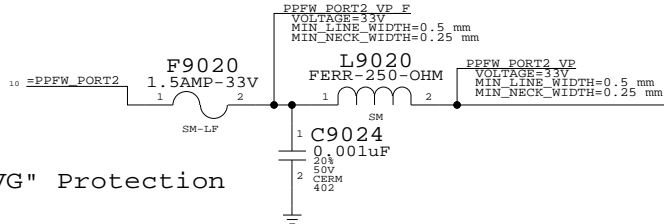


AREF needs to be isolated from all local grounds per 1394b spec

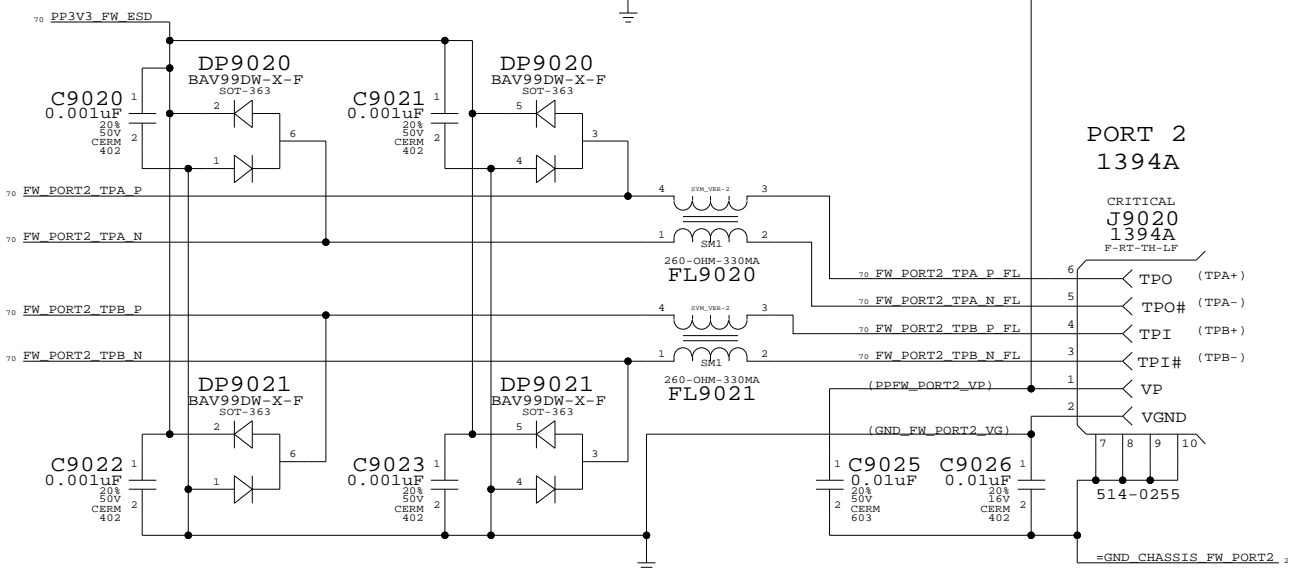
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

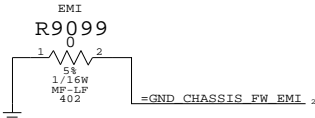
Cable Power



"Snapback" & "Late VG" Protection



PORT 2 1394A



FireWire Ports

SYNC_MASTER=N/A SYNC_DATE=N/A

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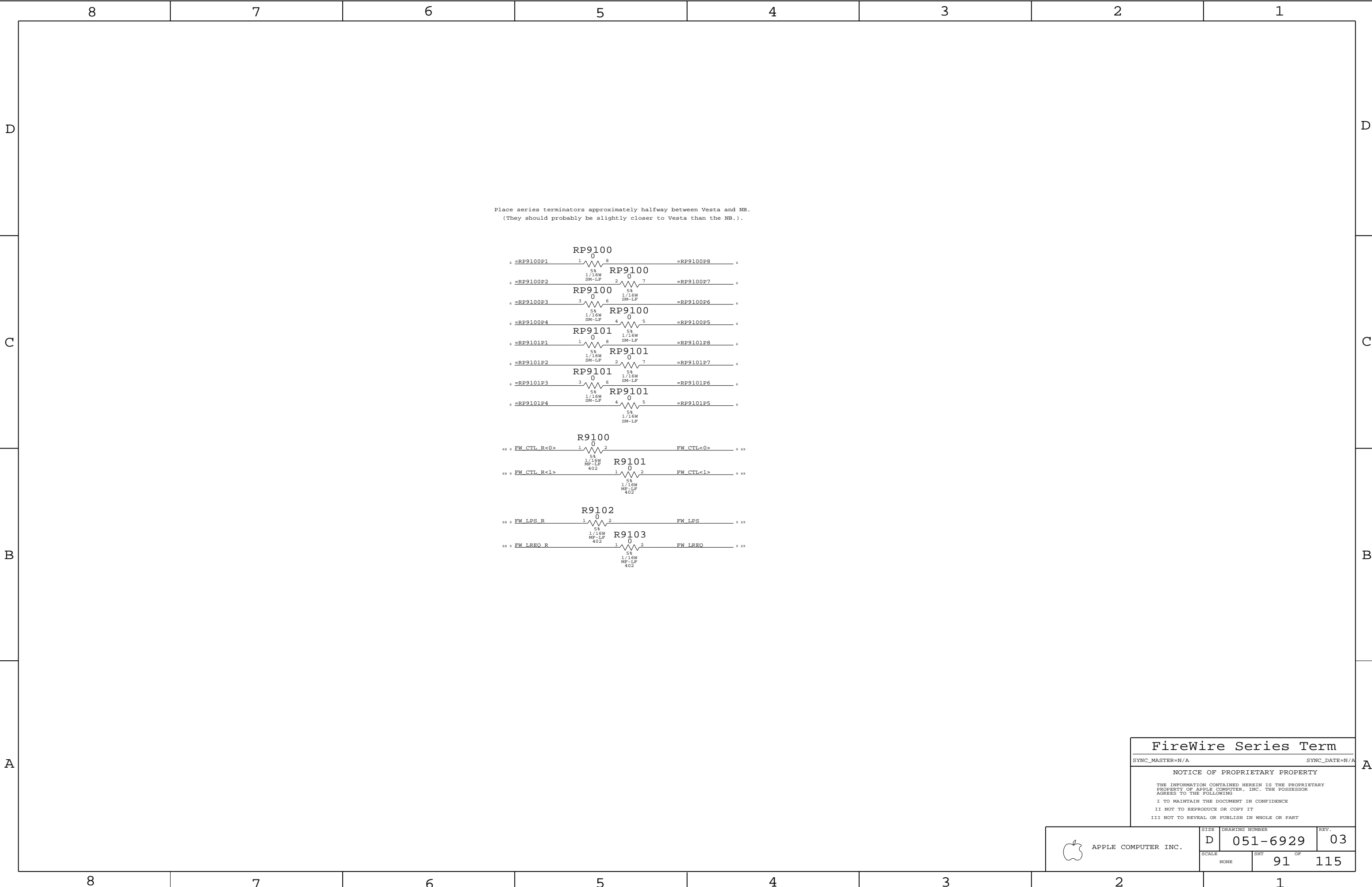
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DRAWING
TITLE=PLASMA
ABBREV=DRAWING
LAST_MODIFIED=Fri Jun 3 15:29:50 2005



FireWire Series Term

SYNC_MASTER=N/A

SYNC_DATE=N/A


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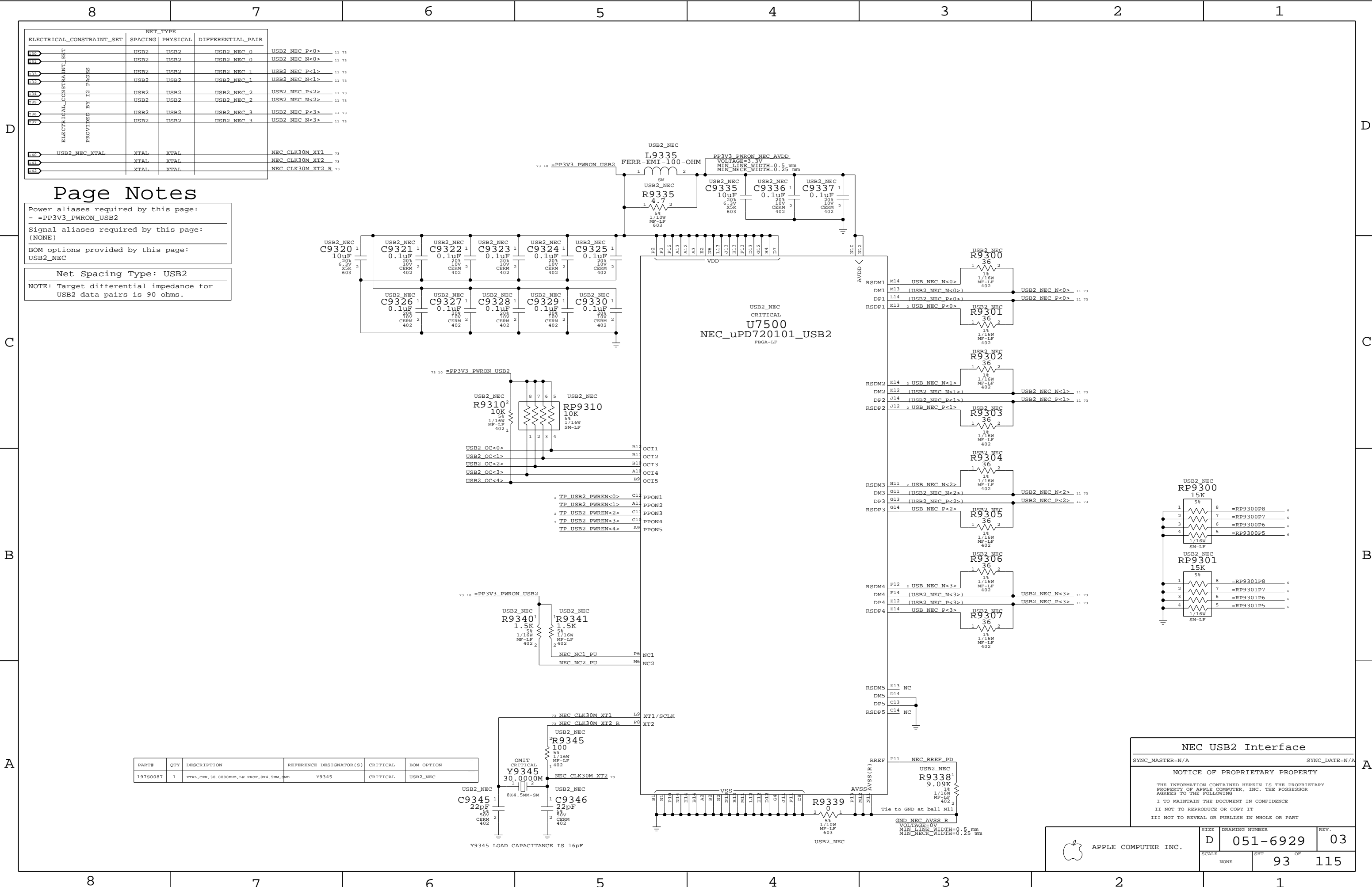
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NONE		91	115	



ELECTRICAL_CONSTRAINT_SET	NET_TYPE				
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
ELECTRICAL_CONSTRAINT_SET PROVIDED BY 12 PAGES	USB2	USB2	USB2_NEC_0	USB2_NEC_P<0>	11 73
			USB2_NEC_0	USB2_NEC_N<0>	11 73
			USB2_NEC_1	USB2_NEC_P<1>	11 73
			USB2_NEC_1	USB2_NEC_N<1>	11 73
			USB2_NEC_2	USB2_NEC_P<2>	11 73
			USB2_NEC_2	USB2_NEC_N<2>	11 73
			USB2_NEC_3	USB2_NEC_P<3>	11 73
			USB2_NEC_3	USB2_NEC_N<3>	11 73
			NEC_CLK30M_XT1		73
			NEC_CLK30M_XT2		73
			NEC_CLK30M_XT2 R		73

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB2

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
USB2_NEC

Net Spacing Type: USB2

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,30.0000MHZ,LW PROF,8X4.5MM,GND	Y9345	CRITICAL	USB2_NEC

NEC USB2 Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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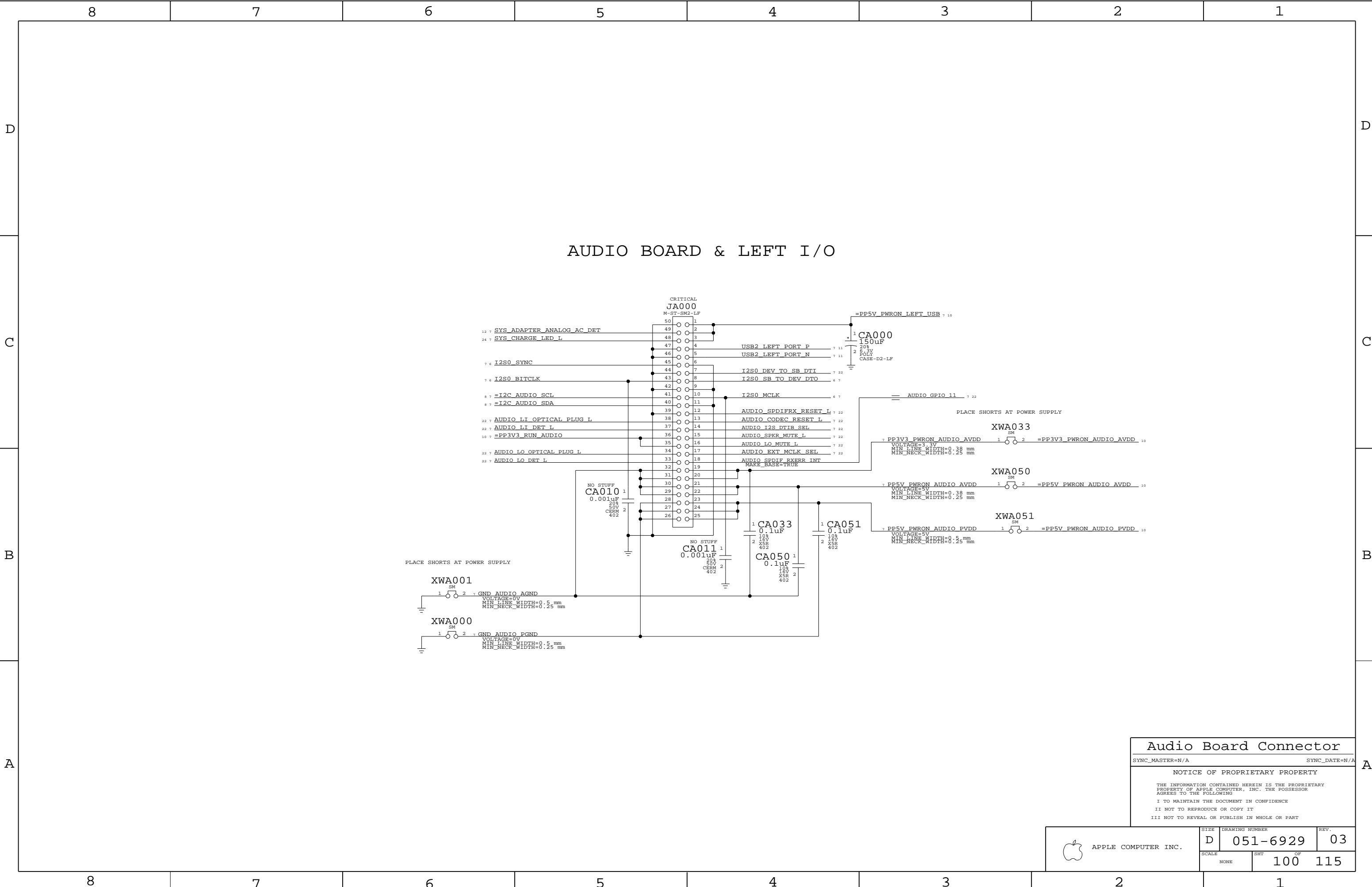
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	NONE	93 115	



Audio Board Connector

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[illegible]

[illegible]

[illegible]

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